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A-5-2 A High Power MOSFET with a Vertical Drain Electrode and Meshed Gate Structure

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A MOSFET has several attractive features as a power device compared with a bipolar transistor. This is because a MOSFET does not exhibit any of the phenomena such as local current concentration, thermal runaway and second breakdown. However, the lack of high current-handling capability and relatively low breakdown voltages have been considered as major obstacles against the realization of a power MOSFET. Recently, Morita et al.[1] proposed a UHF power MOSFET with a vertical electrode geometry which has a high-current capability. Meanwhile, Erb and Dill[2] originated a high voltage MOSFET with an ion implanted offset gate structure, of which a design theory was developed by the authors[3].

In this paper, we present a new type of power MOSFET which has a meshed gate in conjunction with the vertical electrode geometry and the ion implanted offset gate structure, to attain higher power-handling capability. The drain current I_D of several preliminary samples is shown in Fig.1 as a function of the channel aspect ratio W/L, together with the prediction of the design theory. The fact that the experimental I_D is proportional to W/L confirms the absence of local current crowding. It is apparent that a high current device can be obtained when W/L is over 10^5 in the case of P-channel devices. Therefore it is important to make W/L as large as possible for given chip size. The new structure proposed here, shown in Fig.2, has a vertical drain electrode and meshed gate which gives a large W/L per unit chip area. Two distinctive features of structure are as follows: (1) Vertical drain electrode; the drain region is formed vertically while the channel region is still located at the top surface similar to a conventional one. Since the source and the drain electrodes are formed on the top and bottom surfaces respectively, the current can be increased without increase of source resistance resulting in the enhancement of high-current capability. (2) Meshed gate structure; the gate forms a mesh as shown Fig. 2 where the source and drain regions are arranged in a planar checker pattern. This configuration makes it possible that W/L per unit chip area becomes about twice as large as that of a conventional one, and that a gate resistance does not increase even if the effective W increases.

The P-channel device with an ion implanted offset gate structure was fabricated from a N on P^+ epitaxial Si wafer with (100) orientation, using the conventional Si gate technology. Figure 3 shows a photomicrograph of 5° angle lapping for a fabricated device. The photomicrograph of the fabricated device is shown in Fig.4, where the chip size is 5x5 mm. The chip was mounted on a TO-3 package. Figure 5 shows a typical static characteristic of the fabricated device. From this figure, we can see that the breakdown voltage is higher than 85 V. The maximum current is as high as 10 A and the tansconductance is about 1.5 mho. The breakdown voltage is limited by punch-through effect between the bottom drain region and the source region. It is possible

to increase the breakdown voltage by increasing the thickness of the N-type epitaxial layer. Stable operation is obtained even at an elevated ambient temperature of 180°C, due to a negative temperature coefficient of hole mobility in the channel.

Reference

(1) Y.Morita, H.Takahashi, H.Matayoshi and M.Fukuta; IEEE, Trans. ED-21, p.733 (1974).

(2) D.M.Erb and H.G.Dill; IEDM, 21-4 (1971).

(3) I.Yoshida, T.Masuhara, M.Kubo and T.Tokuyama; Proc. 6th Conf. on Solid-State Devices, p.429 (Tokyo 1974).

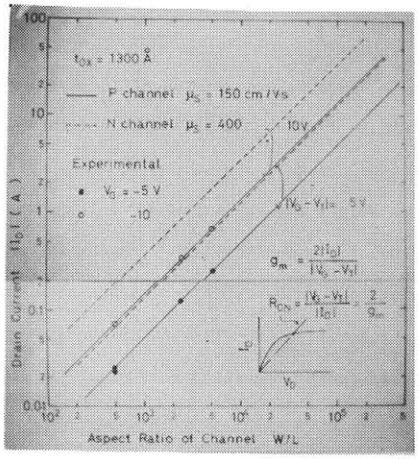


Fig.1 Drain current as a function of channel aspect ratio in the high voltage MOSFET.

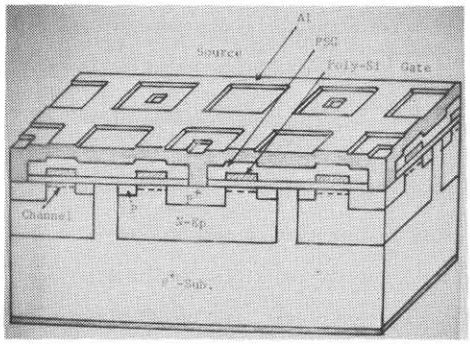


Fig.2 Schematic cross section of the high power MOSFET.

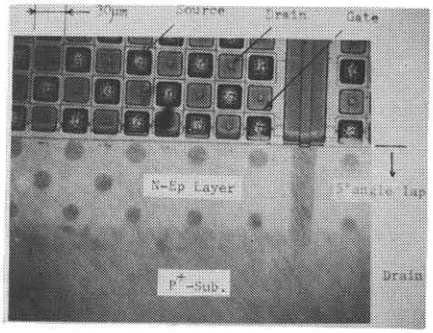
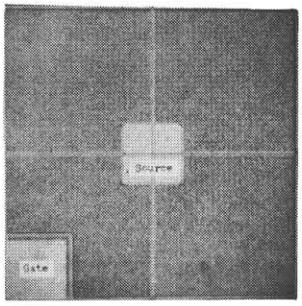


Fig.3 Photomicrograph of 5° angle lapping for the fabricated device.



(5x5 mm)

Fig.4 Photomicrograph of the fabricated device.

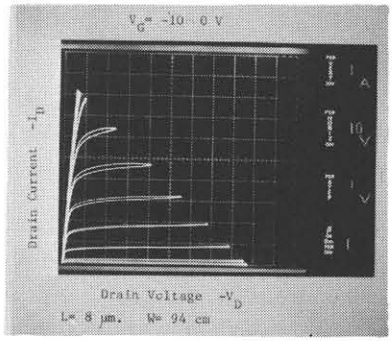


Fig.5 Typical static characteristic of the fabricated device.