

- A-5-3 A 256-b Nonvolatile Static Random-Access Memory
with MNOS memory transistors
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In spite of the rapid progress of recent MOS RAMs (Random Access Memories) in operating speed, bit density and power dissipation, no nonvolatile RAM has been developed which can be operated beyond a practical memory cycles. Several studies on the nonvolatile RAM have been reported,⁽¹⁾⁽²⁾ but none has successfully operated beyond 10^{13} writing cycles because of the degradation of memory transistors.⁽³⁾ This paper presents a nonvolatile static RAM with MNOS memory transistors, which is available for such application areas by means of a new circuits configuration.

Nonvolatile memory cell in our memory consists of flip-flop with MNOS memory transistors as shown in Fig. 1. MNOS transistors MT₁, MT₂ are incorporated in series to depletion mode load transistors, and a switching MOS transistor is connected in parallel to each MNOS transistor to obtain the usual static memory cell operation independent of MNOS transistors. When the negative voltage pulse is applied to the MNOS gate (MG) line, the information of the static memory cell is written into the MNOS memory transistors. At the time of the power on, the read voltage pulse is applied to the MG line and the information of the MNOS transistors is transferred to the static memory cell. The positive voltage pulse is applied to the MG line to erase the information of MNOS transistors. The typical memory characteristics of MNOS transistor are shown in Fig.2.

The block diagram of the developed 256-b nonvolatile RAM using these nonvolatile memory cells is shown in Fig. 3. The word organization of this RAM are 64 words X 4 bits. The memory array is 16 X 16 memory matrix, which is decoded into a 64 X 4 organization by X and Y decoder. Data communication is accomplished through the data circuits and control circuits. The gate electrodes of MNOS transistors are connected to a common control signal MG line. This RAM operates as the usual static RAM under stable power supply. And it can operate as the nonvolatile RAM by applying a control signal to the MG line from the external circuits at the transient of the power supply. Since the number of memory cycles of the MNOS transistors is the same as that of the power OFF/ON cycles, the MNOS memory cycles over 10^5 times are considered sufficient

for the usual application areas.

The devices in this RAM are fabricated on one chip using p-channel silicon gate E/D technology except for the Al gate MNOS transistors. A pattern microphotograph of a fabricated IC chip, $3.0 \times 3.6 \text{ mm}^2$ in size, is shown in Fig. 4.

The typical characteristics of this RAM are : (a) access time is 400 ns, and cycle time is 1 μs , (b) power dissipation is less than 600mW in the normal static RAM mode, (c) both inputs and outputs are TTL compatible except for MG signal, (d) the retention time of the stored data is more than 1 year. The typical output waveform is shown in Fig. 5.

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- (1) J.R.Cricchi et al., IEEE ISSCC Dig. Tech. Papers, pp 204-205 Feb. 1974.
- (2) Y.Uchida et al., IEEE ISSCC Dig. Tech. Papers, pp 108-109 Feb. 1975.
- (3) T.Tanaka and Y.Nishi, Proc. 6th CSSD (1974) pp 203-209, Tokyo.

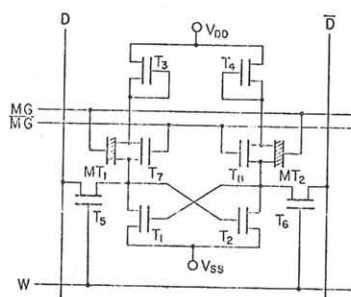


Fig. 1 Circuit configuration of the nonvolatile memory cell.

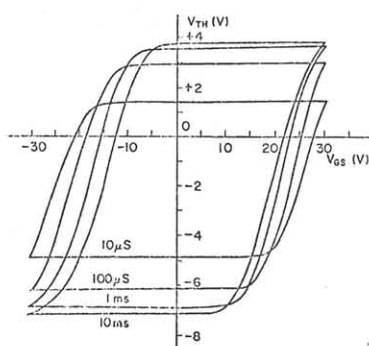


Fig. 2 The memory characteristics of MNOS transistor.

Fig. 5
The typical data
output waveform.

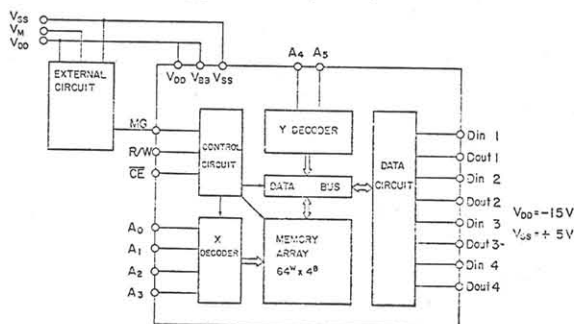
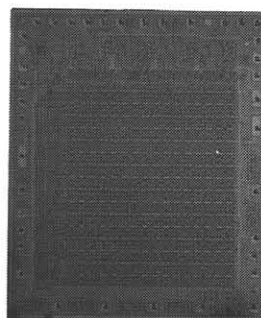


Fig. 3
Block diagram of
the 256-b nonvolatile
static RAM.

Fig. 4
A microphotograph
of nonvolatile static
RAM IC chip.



Address

CE

OUTPUT

