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This paper presents the device design of short channel MOS-FETs based on the accurate two dimensional analysis and some experimental results of the related small size devices providing an ring oscillator IC with 0.66 n sec. gate delay time.

Some works have been done on the two dimensional device analysis of characteristics in short channel devices.^{1),2),3)} Our interests are especially stressed on the effect of the drain diffusion depth and the drain & substrate voltages on the threshold lowering behavior in order to determine the device structure and the operating conditions. The slope of the tailing drain current vs. the gate voltage and the substrate bias coefficients are also of interest. This is because these parameters would not be constant any more in short channel devices and be varied with the vertical and horizontal fields.

A precise MOS-FET analysis program was first prepared.⁴⁾ Some $\log I_D - V_G$ curves computed were compared with the experimental result of a 5 μ m device as shown in Fig. 1 exhibiting the capability of the program as a good design tool. Next, by the extensive use of the program the variations of threshold voltage as functions of the drain diffusion depth X_j , the channel length L and the drain & substrate voltages were examined. Fig. 2 shows an example of the data predicting the effects of decreasing X_j and lowering the substrate bias V_{BB} on the stabilization of threshold voltage.

Following the indication, the structure of the experimental short channel device

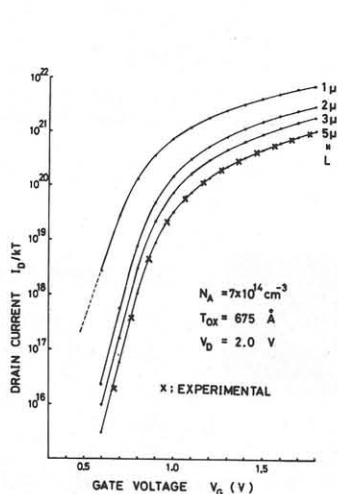


Fig. 1. $\log I_D - V_G$ curves computed with the developed program. Experimented plots of a 5 μ m device are also shown.

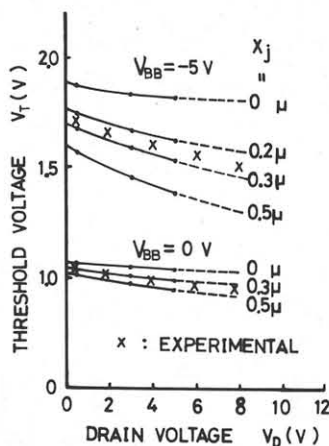


Fig. 2. Variation of threshold voltage with the drain voltage. $L = 2 \mu$ m.

was determined as shown in Fig. 3, where the shallow source & drain layers were formed by implanting phosphor and the gate size L_M (the channel length L) was varied from 2 to 8 μm (about 1.5 to 7.5 μm). Fig. 4 shows some $I_D - V_D$ curves of the ion implanted MOS-FETs. Because of the shallow junction depth of 0.3 μm , a device with 1.5 μm channel length still has a good punch-through break-down voltage of over 10 volts.

The experimental values of the threshold voltage variation vs. the drain voltage are also plotted on Fig. 2 showing a good agreement between computation and experiment. The variation of the substrate bias coefficient as the decrease of the channel length L was first pointed out by computation and then verified by experiment as shown in Fig. 5. It was found that the slope of the tailing drain current vs. the gate voltage tends less steep in a shorter channel device.

A 21 stage E/D MOS type ring oscillator IC composed of the considered 2 μm channel devices was fabricated. A gate delay of 0.66 n sec is obtained from the oscillated waveform shown in Fig. 6.

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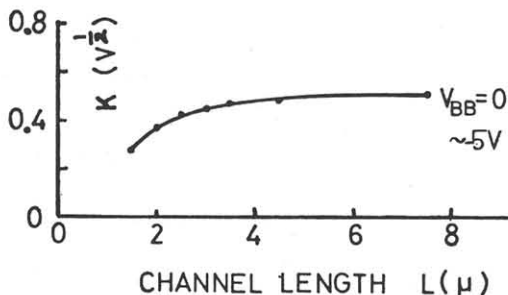


Fig. 5. Variation of the substrate bias coefficient with the channel length L .

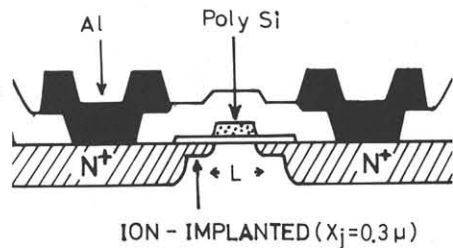


Fig. 3. The Cross-sectional View of the experimented MOS FET with shallow source and drain junctions.

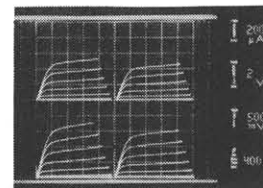
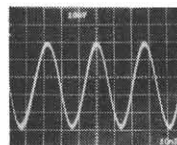


Fig. 4. $I_D - V_D$ characteristics of ion-implanted short channel MOS FETs.



$t_{pd} = 0.66 \text{ ns/stage}$
 $P_d = 0.18 \text{ mW/stage}$
 $t_{pd} \cdot P_d = 0.12 \text{ pJ}$
 $(\beta_R = 2)$

Fig. 6. The output waveform of a 21 stage ring oscillator IC. $L = 2 \mu\text{m}$ and $V_{DD} = 3\text{V}$, $V_{BB} = -3\text{V}$.