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Short Channel, Low Noise UHF MOSFET's Utilizing Molybdenum-Gate

Masked Ion-Implantation

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In recent years, high frequency and low noise MOSFET's are required for the linear amplifiers and TV tuners due to their excellent cross modulation characteristics.

This paper describes the application of ion-implantation to the very short channel FET's and reduction of the high frequency noise using Mo as a gate material.

In the case of small signal operations at high frequency range, the parasitics such as distributed gate resistance or source resistance act as noise sources. The high frequency noise figure of a MOSFET in saturation region is approximately expressed as follows.

$$F \approx F_i + \frac{1}{G_s} \left[|y_{11} + y_s|^2 R_g + (|y_{11} + y_s|^2 + |y_{11}|^2) R_s \right] \quad (1)$$

where F_i is the noise figure of an intrinsic FET and y_{11}, y_s are respectively input and generator admittances. G_s, R_g and R_s are generator conductance, gate resistance and source resistance.

Equation (1) shows that to accomplish low noise figure, minimization of F_i and reduction of R_g and R_s are necessary. The value of F_i can be minimized by shortening the channel length, therefore for sufficiently short channels the last two terms become dominant.

The gate masked ion-implantation method¹⁾ is useful for the short channel FET because of its high punch-through voltage and small overlap capacitance. On the contrary, implanted layer acts as an extrinsic source resistance and this resistance can be decreased with increasing annealing temperature. In addition to the source resistance, the width of the gate stripe must be as small as the channel length, hence distributed gate resistance arises. The poly-Si film is good for high temperature annealing but its sheet resistance is rather high. On the contrary, the Mo film is superior for its low resistivity and high melting point.

To confirm this idea, n-channel devices with dual-gate structure were fabricated on 3-5 Ω cm p-type (100) Si substrates. Conventional methods were used for source, drain contact diffusion and gate oxidation. The Mo film was deposited by RF sputtering on an 0.06 micron-thick gate-oxide and chemically etched into 2-micron gate stripes by high resolution photolithographic techniques. Source and drain shallow layers were formed by 5×10^{14} phosphorus ions/cm² implantation at 100 KeV through gate-oxide, then annealed at 900 °C for 20 min. in N₂ followed with 400 °C, 1 hr annealing in H₂ which reduces surface-states generated during high temperature annealing.

Figure 1 shows the schematic cross section (upper) and its microsection (lower) of the n-channel device where the implanted regions extend the diffused contact regions and are automatically registered with respect to the gates.

Figure 2 shows the noise figure as a function of gate-oxide thickness measured at 800 MHz.

In this figure, the variation of noise figure is slight and the optimum value of the gate-oxide thickness is between 0.05 and 0.07 microns.

Figure 3 shows the noise figure measured at 800 MHz as a function of the channel length, together with theoretical calculation. In this figure, the experimental data of the noise figure agreed with the theoretical predictions except the shorter channel region below 1 micron. In this very short channel region, the noise figure increases with decreasing the channel length and this effect is attributed to the punch-through current which increases significantly with decreasing the channel length.

Throughout these experiments, the lowest noise figure, ever reported, of 2.4 dB with 20 dB power gain was achieved and the cross modulation of the FET-tuner improved over 10 dB than that of a bipolar transistor.

Reference

- 1) BOWER R.W. et al ; IEEE Trans. on ED, ED-15, NO.10, pp757-761, Oct. (1968)

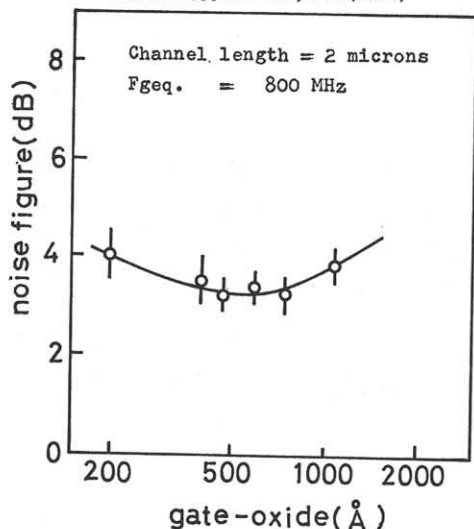


Fig. 2 Noise figure vs. gate-oxide thickness at 800 MHz.

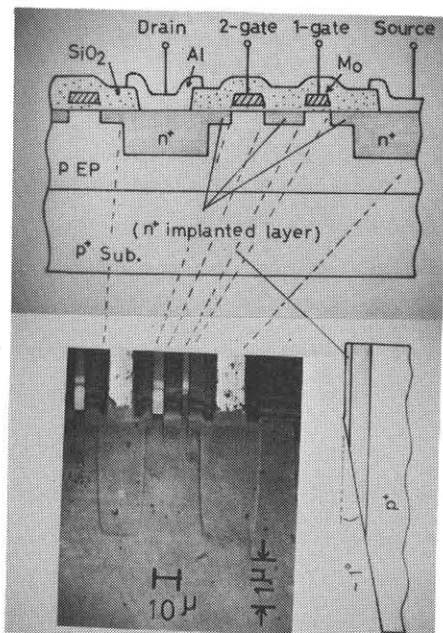


Fig. 1 Schematic cross section and its microsection of the n-channel device made by implantation.

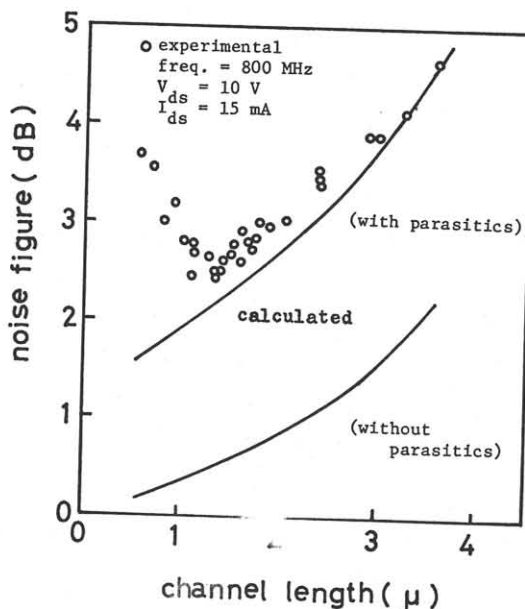


Fig. 3 Noise figure vs. channel length at 800 MHz.