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A-6-3 VARIABLE DISTRIBUTION PARAMETER FIELD EFFECT DEVICES

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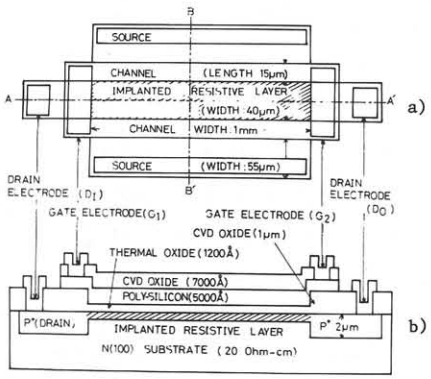
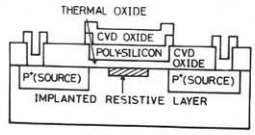
A new field effect device called the Variable Distribution Parameter-Field effect device(VDP-FED), whose distribution parameter can be continuously varied as a function of the applied gate voltages, has been proposed and developed. This VDP-FED essentially manifests a new functional device with both characters of the semiinsulated resistive gate field effect device[1] and the continuously variable threshold voltage device[2].

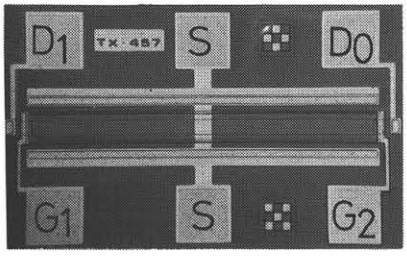
The purpose of this paper is to investigate the basic principles, device structures and electrical characteristics in the VDP-FED. Furthermore, this paper will also describe some possible and useful applications for the gain control circuits.

Device Model and Structure:

A typical device structure, photograph and symbolmark of the VDP-FED are shown in Fig. 1. The VDP-FED has a special device structure which is composed of the semi-insulated polycrystalline resistive gate with two gate electrodes of G_1 and G_2 to create a potential difference in between and the implanted high resistive drain layer with two drain electrodes of D_1 and D_0 as the signal input and output. The drain layer consists of the boron implanted shallow junction having the high sheet resistance of 800 Ω/□. The energy and surface impurity density of ion implantation used in this experiment were 50 KeV and 1×10^{14} cm^{-2}, respectively.







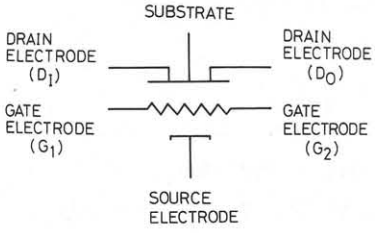


Fig. 1: Device structure of VDP-FED.

a) Plane view.

b) Horizontal cross-sectional view for A-A' line of Fig. 1 a).

c) Vertical cross-sectional view for B-B' line of Fig. 1 a).

d) Photograph of device.

e) Symbolmark.

Experimental Results:

Using the VDP-FED under the bias conditions as shown in the inset of Fig. 2, the continuous variation of distortion parameters, specifically the locational dependence of channel resistance and the distribution resistance in drain layer, will be created. In Fig. 2, a typical characteristic of the logarithmic attenuation against linear gate voltage, as a parameter of the various gate voltage difference of $V_{G2}-V_{G1}$ at the input signal of 1 KHz and -10 dBm in p-channel device, is shown as an experimental result.

In case of the zero voltage difference ($V_{G2}-V_{G1}=0$), an attenuation characteristic in the logarithmic scale indicates a linear dependence on the reciprocal square root of the gate voltage.

On the other hand, when a voltage difference($V_{G2}-V_{G1}<0$) is present, the linear gain attenuation of more than 70 dB in the logarithmic scale were measured.

Furthermore, in Fig. 3, the observed results of the total harmonic distortion against the input signal frequency are shown as a parameter of various gain attenuation at an input signal of -10 dBm. In addition to these basic characteristics, the theoretical analyses and consideration of the VDP-FED will be presented in detail.

As a conclusion, the VDP-FED will be useful for the logarithmic amplifier or the extremely wide dynamic range compensator such as a signal compressor and expander. Applications of the devices will also be reported in detail.

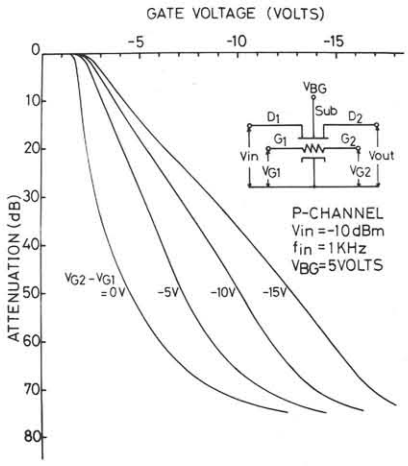


Fig. 2: Characteristics of gain attenuation against gate voltage as a parameter of gate voltage difference at an input signal of 1 KHz and -10 dBm.

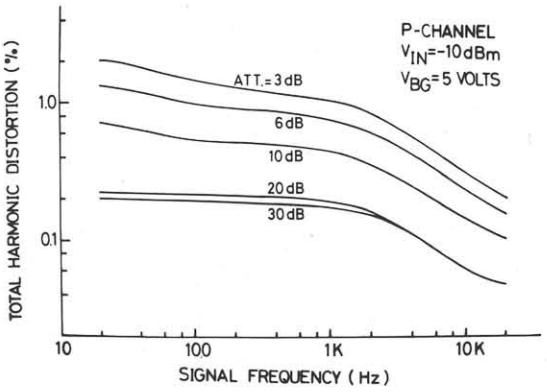


Fig. 3: Characteristics of total harmonic distortion against input signal frequency as a parameter of the various gain attenuation.

References

1) T.Yamada,Y.Hirata and S.Sato: 1974 IEDM Technical Digest,pp.533-536.

2) T.Yamaguchi and S.Sato: 1974 IEDM Technical Digest,pp.537-540 and The Proceedings of 6th Conference on Solid State Devices in 1974,Tokyo,pp.107-116.