

S. Onga, T. Yoshii, K. Hatanaka** and Y. Yasuda
Toshiba R and D Center, Tokyo Shibaura Electric Co., Ltd.

Kawasaki, Japan

**Faculty of Science, Gakushuin University

The usefulness of silicon films on sapphire (SOS) for fabrication of integrated circuits have demonstrated. One of the advantages of SOS over bulk silicon is the fabrication of high speed low power integrated circuits because of a reduction of parasitic capacitance. It is, however, a disadvantage of SOS that effective mobilities in n-channel MOS transistors are lower than those of bulk silicon.⁽¹⁾ The lower mobilities are thought to be mainly due to high densities of crystal defects and residual compressive stress⁽²⁾ in silicon films. The purpose of this paper is to describe and discuss effects of the defects and residual stress on electrical properties of n-type (001) silicon films on (1012) sapphire, especially related to the anisotropy of electrical properties in the film and to the in-depth characteristics.

Hall measurements were made on Hall bridges with the current directions along [110] $[1\bar{1}0]$ and [100] of silicon films, 1 μ m thick, doped with phosphorus at concentrations ranging from low $10^{16}/\text{cc}$ to high $10^{18}/\text{cc}$. A significant anisotropy is found in resistivity of SOS. The anisotropy in the (001) plane can be partly accounted for through the piezoresistance effect of thermally induced stress due to the difference in thermal expansion coefficients between silicon and sapphire.⁽³⁾ However, there exists another new anisotropy in electrical properties of SOS at lower carrier concentration, as shown in Table 1. These two specimens along the [110] and $[1\bar{1}0]$ silicon direction must be subject to an identical thermal stress. This anisotropy can be explained by dislocation arrays characteristic of the silicon film. Figure 1 shows a typical image of etch pit patterns in the film surface using Dach etch technique. This figure reveals arrays of dislocation pits showing low angle grain boundaries. It should be noted that the dislocation arrays along the [110] direction are preferential to those along $[1\bar{1}0]$. Thus electrons transported along $[1\bar{1}0]$ meet with the boundaries more frequently than ones along [100] do. On the other hand, at higher carrier concentrations, the above-mentioned difference is not found, because

*Apart of this work accomplished under the contract with the Agency of Industry, Science and Technology for the Research and Development of a Pattern Information Processing System.

there is not the overlaps among cylindrical space charge regions around dislocations. Consequently, it is concluded that the mobility anisotropy is due to the scattering in space charge walls around the grain boundaries. This scattering mechanism has been investigated in more detail by the temperature dependence of Hall mobilities in the two $\langle 110 \rangle$ directions (Fig. 2). The mobility difference between the two directions becomes more remarkable at lower temperatures, since the space charge scattering is more predominant.

Moreover, we have studied the in-depth profile of Hall mobility and carrier concentration in a $1\mu\text{m}$ -thick, n-type SOS film using deep-depletion-type MOS Hall devices (Fig. 3). Observed Hall mobility decreases with distance from oxide interface. This decrease is more rapidly at Liq N_2 temperature. Furthermore, a detailed study is made of film thickness dependence of dislocation density through etch pit counts on surfaces of silicon films in the thickness range of 0.1 to $1.0\mu\text{m}$ (Fig. 4). The densities are found to vary at $t^{-0.7}$ with thickness (t). On the other hand, precise X-ray measurements of the silicon lattice constant at various thicknesses indicate that the compressive strain dose not depend on thickness. Consequently, these results lead to the conclusion that the dislocation scattering is responsible for the mobility decrease in Fig. 3. As for scattering mechanisms and more details connected with the crystalline imperfections in SOS, we will report at the conference.

References:

- (1) H. Tango et al., Proc. 6th CSSD (1974). Japan Soc. Appl. Phys., (Tokyo, 1975) 225.
- (2) J. Hyncek, J. Appl. Phys., **45** (1974) 2631.
- (3) A. J. Hughes et al., J. Appl. Phys., **44** (1973) 2304.

Table 1

C-61		R.T.	
Resistivity ($\Omega\text{-cm}$)	Carrier Concentration ($1/\text{cm}^3$)	Hall Mobility ($\text{cm}^2/\text{v}\cdot\text{sec}$)	
[110]	0.6253	2.03×10^{16}	493
[110]	0.8743	1.52×10^{16}	470

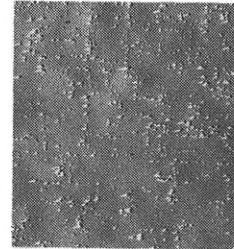
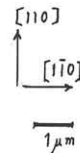
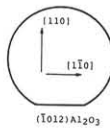


Fig. 1

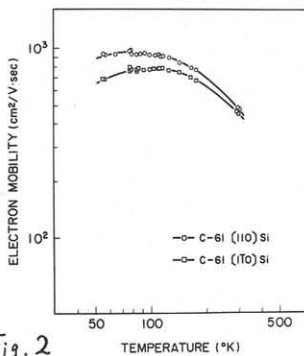


Fig. 2

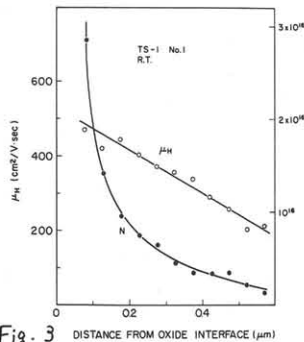


Fig. 3

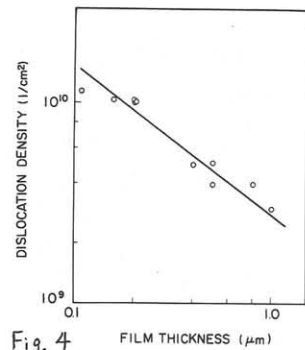


Fig. 4