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B-2-2 10 kbit Bubble Memory Chip : Design and Fabrication

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A 10 kbit bubble memory chip has been developed using 6 μm bubble materials. Some new circuit elements, such as, deformed H transfer-gates and a chevron bubble splitter, were employed, and configurations of bubble control patterns were optimized to obtain a sufficient operating margin and good process yield at the same time. 256 chips were processed and so high process yield as 37.9 % was obtained.

Fig. 1 shows the design of Permalloy and conductor patterns. The major-minor organization, nucleation generator and thick-film serpentine detector are similar to those described by Bonyhard et al. [1]. As shown in Fig. 2, however, the deformed H transfer-gates and the chevron bubble splitter are employed in place of the dollar-sign transfer-gates and the replicator, respectively, and two serpentine detectors are placed side by side to obtain good noise cancellation. In order to attain good process yield the minimum pattern gap was determined to be 2 μm in both Permalloy and conductor patterns, and one minor loop was spared for a redundant loop. The period, bar width and pattern gap of the T-bar patterns in the minor loops are 28 μm, 4 μm and 2 μm, respectively. The chip size is 3.3 x 4.3 mm.

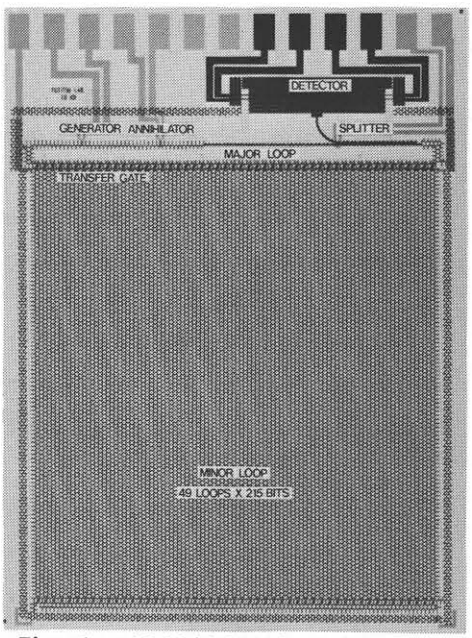

Fig. 1. 10 kbit bubble memory design.

The chips were fabricated by the conductor first process [1]. Bubble materials are 6 μm $(YSm)_3(FeGa)_5O_{12}$ epitaxial films and hard bubbles are suppressed by ion implantation. The chip fabrication process is as follows; (1)sputter a 3000 Å SiO_2 film, (2)evaporate a 4000 Å AlCu film, (3)delineate conductor patterns by

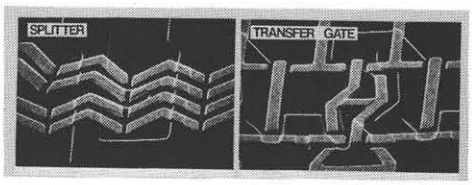

Fig. 2. Transfer gate and splitter.

ion milling, (4)sputter a 9000 Å SiO_2 film, (5)evaporate a 4000 Å NiFe film, (6)delineate propagation patterns by ion milling, and (7)remove SiO_2 from bonding pads by plasma etching.

An example of the bias margin curve at 100 kHz is shown in Fig. 3. The upper margin is determined by 1 mV output signal (5 mA current) in the detector and the lower margin is determined by the bubble strip-out during propagation in the major loop or through the transfer gates. This bias margin curve was further analyzed using a diagnostic test system and the long-term stability of stored data within this margin was confirmed [2].

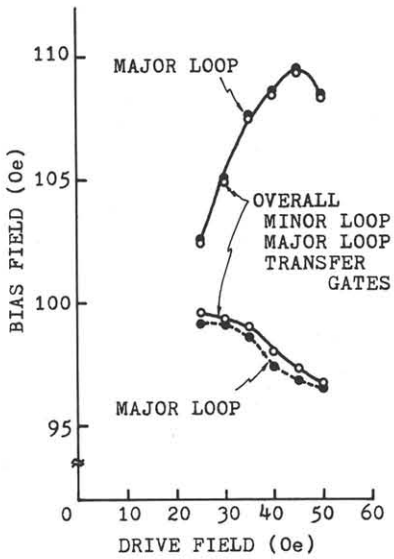

Fig. 3. Example of bias margin curve at 100 kHz.

256 chips (32 wafers) were processed and 97 chips (62 chips without defective minor loops and 35 chips with one defective loop) passed the final testing (more than 4 Oe bias margin window at 40 Oe drive field), and 37.9 % process yield was obtained. The bias margin window distribution of good chips is shown in Fig. 4.

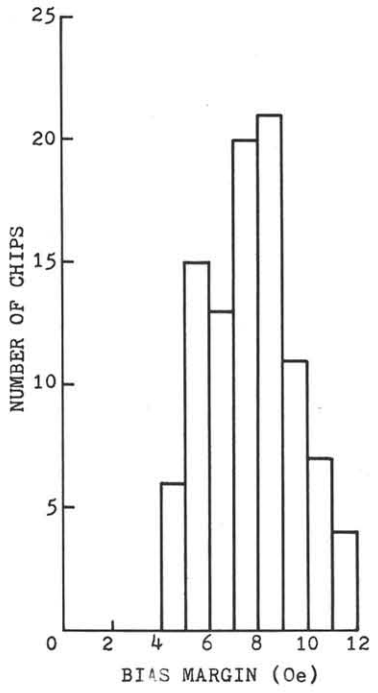

Fig. 4. Distribution of bias margin windows at 40 Oe drive field.

The cause of bad chips was analyzed and the results make us believe that still higher process yield can be obtained for 6 μm bubble chips and reasonable process yield can be expected for 3 μm 100 kbit chips.

1) P.I. Bonyhard et al., "Magnetic Bubble Memory Design," IEEE Trans Magn., Vol. MAG 9, pp. 433-436, September 1973.
2) S. Orihara et al., "Diagnostic Testing of a 10 kbit Bubble Memory Chip," Intermag Conference 6-7, London, 1975.