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A new bipolar type semiconductor device is proposed, manufactured only two diffusion processes and without isolation technique. The device has the n^+ -diffused small electrode instead of the gate electrode in the MOS transistor structure. Some current amplification modes, switching mode, J-FET mode, and punch through mode can be observed. The high photo sensitivity of the device in the charge storage mode operation is applied to the PCD image sensor.

Figure 1 shows the basic structure and the name of each electrode. As shown in this device structure, this device has a small n^+ -electrode instead of MOS gate in MOS transistor. Several phenomena in this device such as, high-low junction effect and spreading resistance effect in the gate electrode and the punch through effect between the emitter and the collector, applied to many modes of operation.

When each electrode potential is biased as shown in Fig. 2, the lowest potential area in the substrate is formed around the n^+ -electrode by spreading resistance of it and so-called high-low junction between the substrate and the n^+ -gate electrode. This area is called a channel. When the channel length is narrow enough and the resistivity of the substrate is high, the channel is nearly punched through and almost all minority signal current injected from the emitter to the channel flows into the collector without recombination at the boundary of n^+ -electrode and the channel, because a high electric field is induced in the channel. On the basis of these phenomena, controlling the gate electrode potential operates PNP type transistor action between the emitter (P), the channel (N) and the collector (P), and switches on and off between the emitter and the collector. Figure 3 shows the current amplification operation and Fig. 4 shows the switching operation of this device. Because of the majority carrier current I_B , the current gain I_E/I_G may be quite small. If the channel is completely punched through, I_B may be zero and punched through threshold

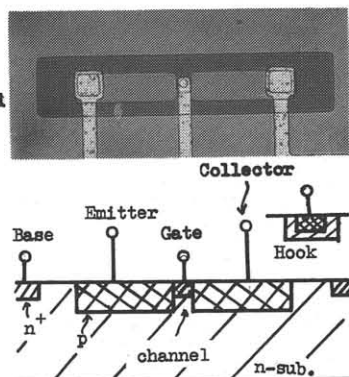


Fig. 1 Device structure

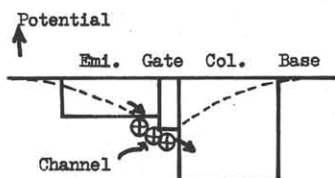


Fig. 2 Potential profile in transistor mode

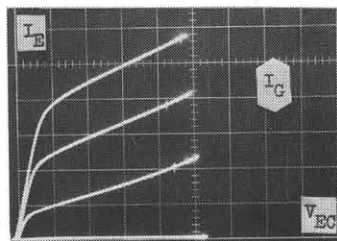


Fig. 3 Current amplification characteristics in transistor mode $V_{EC}: 1V/div$, $I_E: 0.2mA/div$, $I_G: 1mA/step$.

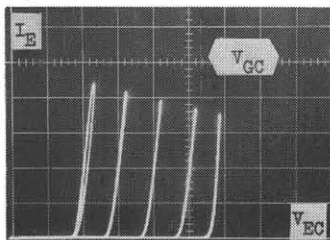


Fig. 4 Switching characteristics in the transistor mode $V_{EC}: 1V/div$, $I_E: 0.2mA/div$, $V_{GC}: 1V/step$.

voltage can be controlled by gate electrode. PNP and NPN complementary transistor structure are formed with hook collector showing in Fig. 1.

On the other hand, when each electrode potential is biased as shown in Fig. 5, unijunction transistor like current amplification operation is realized. Figure 6 shows this amplification characteristics. The high current gain is available owing to the conductivity modulation of the spreading resistance of the n^+ -electrode by means of the carrier accumulation.

When each electrode potential is biased as shown in Fig. 7, J-FET type operation is observed as shown in Fig. 8. In the mode, the base and the gate correspond to the source and the drain of J-FET respectively, and the emitter and the collector correspond to the gate of J-FET.

This device has high photo sensitivity in the charge storage mode operation controlling the gate potential similarly the MOS transistor. For this purpose, the emitter is floated electrically and the emitter-substrate pn junction is employed as a photo diode and as a charge storage capacitance. Figure 9 shows the waveforms of the storage mode operation in the device with hook collector. The charge storage time is 10 msec and the illumination intensity is about 100 Lux.

The devices on one substrate may be isolated each other by the base electrode because the base electrode potential is always higher than another regions and minority carriers flows through the emitter, the gate and the collector locally. Then high integrated logic circuit are available by combining I^2L and PCD. For example, by combining this device array as a photo sensor with the PCD scanner, it can compose a highly sensitive imaging device. The 128 bit linear image sensor has been composed and reported in this issue.

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Reference:

- (1) T. Suzuki and Y. Mizushima: Proc. 3rd CSSD, Tokyo, Japan (1971) J.J.A.P. (1972) 40, Digest of Technical Papers ISSCC (1972) 28
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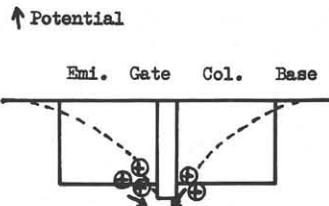


Fig. 5 Potential profile in UJT mode

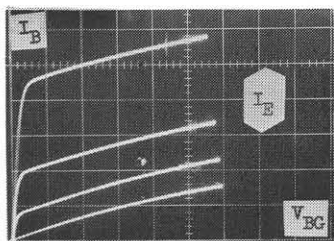


Fig. 6 Amplification characteristics in UJT mode. V_{BG} : 1V/div. I_B : 0.2mA/div. I_E : 10, 20, 50 μ A

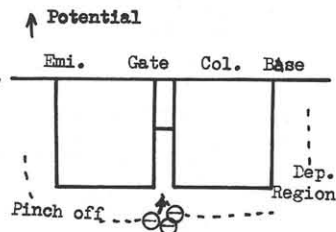


Fig. 7 Potential profile in J-FET mode.

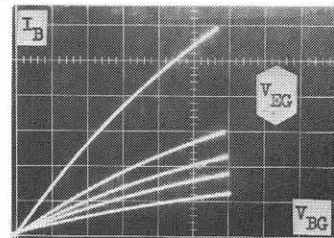


Fig. 8 Voltage controlled characteristics in the J-FET mode. V_{BG} : 1V/div. I_B : 50 A/div. V_{EG} : -5V/step.

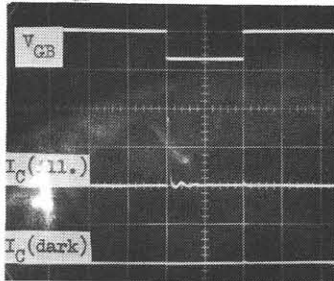


Fig. 9 Storage mode operation

V_{GB} : 5V/div. I_C : 0.1mA/div. t : 5 μ sec/div.