Digest of Tech. Papers The 7th Conf. on Solid State Devices, Tokyo, Sep. 1975

E-2-1 Physical and Technological Limits in Size of Semiconductor Devices

Takuo Sugano

Department of Electronic Engineering, the University of Tokyo

3-1, Hongo 7chome, Bunkyo-ku, Tokyo 113

Limits in size of bipolar and MOS field effect transistors, which are commonly used in integrated circuits, will be briefly discussed from physical and technological viewpoints. Discussion from economical viewpoints will be not included.

Principal Physical Limits

(1) Edge Uncertainty(1)

In lithography edge uncertainty of the order of the wave length should be assumed. This can be understood as diffraction phenomenon and also from Heisenberg's uncertainty priciple, which gives the uncertainty in location ΔL,

$\Delta L \geq \frac{\lambda}{2}$ (1) Equation (1) means that the uncertainty in location for visible light is about 0.5 μm, which has been attained experimentally. The uncertainty for electron beam accelerated by 10^2 - 10^3 volt is 10^{-1} - 10^{-2} nm. With heavy ion beam extremely small uncertainty can be obtained.

(2) Fluctuations of Dopants Numbers(1)

The statistical fluctuations of dopants numbers are unavoidable and become large when the size of a particular region in a semiconductor is small and the number of doping atoms is small. Let N_o be the mean number of impurities per cubic element, ε be the maximum allowed fractional deviation from the mean, the fraction of cubes S in which ε is exceeded may be obtained from

$S = 1 - \frac{2}{\sqrt{2\pi}}\int_0^{\varepsilon N_o^{1/2}} e^{-\frac{y^2}{2}} dy$ (2) where $y = (N - N_o)/\sigma$ and σ = standard deviation = $N_o^{1/2}$ Results of calculation show that even if 10 % tolerance allowed, failure rate S is 2×10^{-3} for $N = 10^3$ and less than 10^{-8} for $N = 10^4$.

(3) Saturation of Drift Velocity of Carriers

Saturation of drift velocity of carriers limits the maximum current density. Assuming the saturation velocity as 10^7 cm/sec, the maximum current density in silicon can be calculated as 10^3 A/cm^2 - 10^6 A/cm^2 for 10^{15}/cm^3 - 10^{18}/cm^3 of carrier concentration. The transfer conductance of bipolar transistors are proportional to the collector current I_c, that is, $\frac{qI_c}{k_BT}$ To get the transfer conductance of 1 m$\mho$ the collector current of 25 μA and therefore the collector cross-section of 2.5 μm^2 is required. The transfer conductance of MOSFETs is largely determined by geometrical factor and the gate voltage and not by the drain current. However the drain current I_D is given by $I_D = qv_{ds}nw$ where v_{ds} is the saturation velocity of carriers in the channel, n is the carrier density per unit channel area, and w is the channel width. n is limited by the breakdown field strength in SiO_2 and less than $10^{12}/cm^2$. Again assuming v_{ds} is 10^7 cm/sec, the minimum channel width for the drain current of 1 μA is of the order of 10^{-2} μm.

Principal Technological Limits

(1) Scattering of Beam in the Resist[1]

The beam spread can be assumed to be comparable to about half the penetration range, that is, the thickness of the resist film. The thinnest possible layer is several molecules thick and would be 25 Å thick. Therefore technological limit of edge uncertainty is determined by thickness of resist and of the order of 20 Å.

(2) Device Characteristics

It is recognized that the practical limitations of size of MOSFETs is gate oxide breakdown and drain-source punch through.[2]

The minimum oxide thickness gives the maximum substrate doping concentration and also the minimum channel length to avoid the punch through phenomenon. The minimum oxide thickness should be thicker than 50 Å to avoid tunneling of carriers through the oxide and this gives 0.2 μm for the minimum channel length. However the punch through phenomenon can be avoided by using lightly doped drain region. Of course appropriate scaling for depth of source and drain junctions should be done.[3]

In bipolar transistors the minimum base region thickness is determined by punch through.[4] The thickness is essentially important for high speed operation of the devices, however from view points of packing density the substrates are sufficient-ly thick, so the thickness limitation is rather out of interest.

Size limit due to edge uncertainty and effect of beam scattering in lithography is far beyond the present technology limit. The most serious, essential limit is given by the statistical fluctuation of dopants numbers.

Saturation of drift velocity gives the limit for cross-sectional area of bipolar devices.

References

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