

E-2-2 Limit of the Microelectronic Fabrication

Kazumasa ONO

Musashino Electrical Communication Laboratory

Nippon Telegraph and Telephone Public Corporation, Musashino, Tokyo.

Approaches to the finer pattern and the higher density are continued in the large scale integration technology.

The major items which limit the LSI fine integration are such as

- 1) materials
- 2) technologies (experiences)
- 3) equipments (performances, efficiencies)
- 4) tools (efficiencies)
- 5) measurement techniques, assessments
- 6) process environments.

Table 1 shows the key problems of microelectronic fabrication processes. In the wafer process, photolithographic process affects the minimum length of fabrication. Table 2 shows the limitation factors in the photo resist process. This is the estimation not from the theoretical but from the experiences.

The electron beam and X-ray lithographic processes are not yet in production but looking for the favourite system in the future lithographic technology.

By means of this technology, minimum stripe width may be less one order compete

Technology	Present condition	Items of investigation	Remarks
Impurity doping	1) Ion implantation 2) Thermal diffusion	1) Automation 2) Maskless method	Surface concentration and depth.
Isolation	1) Dielectric isolation 2) Air isolation 3) Junction isolation	1) New isolation technic 2) Reduction of isolation area	Dielectric isolation are most usefull.
Thin film	1) Yield 2) Pin-hole	1) Isotropy of thickness 2) Gate metal materials 3) Stability 4) New film materials	300 Å films are really needed.
Etching	1) Chemical etching 2) Physical etching	1) Automation 2) Establishment of dry process	Wet and dry process alike.
Crystal	1) Unisotropy	1) Assessments 2) Large wafer 3) Complete crystal 4) Epi wafer	Related on the fabrication process.
Conductor line	1) Double conductor line 2) Surface flatness	1) Multi electrode 2) Conductor material 3) Reduction of conductor line and spaces	Isolation layer material investigation

Note) These technologies mentioned above rely on each other and not independent accurately.

Table 1 : Problems in microelectronic fabrication processes.

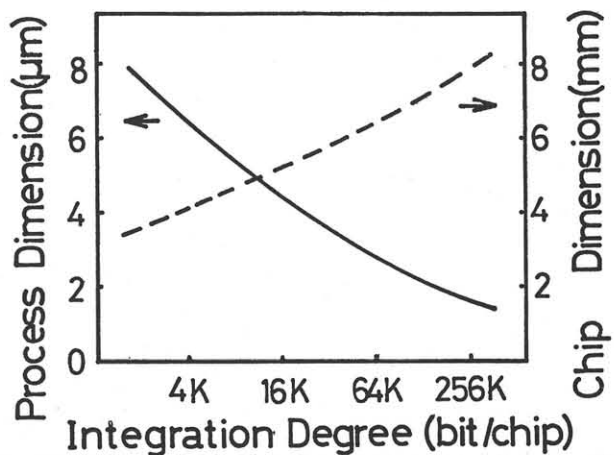
with the ultra violet lithography.

Many limiting factors of microelectronic fabrication processes were mentioned above. But another problems are complexly dependent with LSI fabrication such as the quality of substrate, fabrication apparatus which are largely rely on the import, the measurement and assessment of highly integrated devices, environment of process room and so on. Nevertheless, these problems are tackled and solved for the further development of LSI.

Limiting the attention to the high integration, the solution is not only fine process but also large scale chip dimension. Figure shows the estimation example of integration degree for 1 transistor type MOS memory which implies on the surrounding circuitry.

In this figure, process dimension and chip dimension are also variable.

Conclusively, for reallization of ultra LSI as announced now, it should be needed to rearrangement and to improve of usual technologies and to develop the new microprocess technologies.



Items	Precision		Limiting Factor	Remarks
	Present	Limit		
Resolution of photo resist	±0.1μ or less	±0.1μ or less	Dimensions of resist polimer	
Masks	0.5	0.2	1) Precision of repeater 2) Mask materials	Depended on area
Mask alignment manual automation	1 1	0.2 0.25	1) Precision of aligner 2) Skillness	Individual variation must be considered in manual case.
Bruring in exposure process	0.5	0.25	1) Resist thickness 2) Planability of wafer 3) Reflection of mask 4) Resist material 5) Exposure time 6) Development time	Counter measures for reflection at mask or wafer are working out.
Synthetic number	1.5	0.5		
Minimum stripe width	4	2		Contact type note)

Note) For reduction projection type, there are some problems in manufacture base, because of repeat formula. Nevertheless, 1 to 1.5 micron minimum stripe width are produced.

Table 2 : Ultra violet lithography precision