Digest of Tech. Papers The 7th Conf. on Solid State Devices , Tokyo, Sep. 1975

E-2-3 Note on Limitations in MOS LSI's from a Design Viewpoint

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Along with recent rapid progress towards high density integration of semiconductor devices, one pays attention to the fundamental limitations by various physical phenomena[1-5]. Hoeneisen and Mead[1] proposed a silicon-gate MOS transistor of minimum size in MOS LSI's from a fundamental design viewpoint. In their discussion are neglected effects of device temperature and scattering in channel length, both of which are basically important to determine the minimum device size in LSI's. On the other hand, Dennard et al[3] present a device scaling principle on a basis of present day MOS transistors used in MOS LSI's. The scaling approach is well generalized but the scaling relationship cannot be applied exactly for a gate threshold voltage (V_T). Deviation from the relationship in case of low resistivity substrate should be noted especially for a short-channel MOS device of a low supply voltage.

Here we discuss the limitations of MOS LSI's from a similar design viewpoint but by taking into consideration the effects of temperature rise of the device and its nonuniform distribution on the chip and also the effects of scattering in channel length of actual devices on the chip.

The most important parameters in MOS LSI design are channel length (L), thickness of gate oxide (T_{ox}), substrate impurity concentration (N_A) and supply voltage (V_{DD}). These parameters are related to one another through gate breakdown, drain avalanche breakdown, gate turn-on characteristics and so on. We propose a method to determine values of T_{ox}, V_{DD}, N_A and L, which is schematically shown in Fig.1. At first T_{ox} is assumed and then V_{DD} is taken as high as possible under the conditions of A (see Fig. 1), in order to obtain the shortest switching time. N_A and L are also determined considering successively the condistions B and C. The results are as follow:

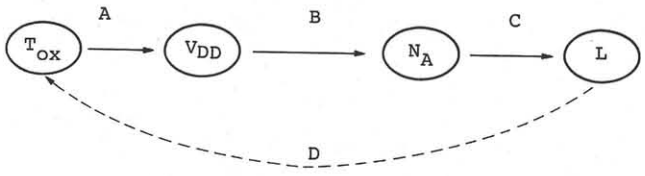
$T_{ox} \simeq 100$ Å,

$V_{DD} \simeq 3$ V,

$N_A \simeq 5 \times 10^{16}$ cm^{-3},

$L \simeq 0.35$ μm

Other parameters such as diffusion depth, distance between two diffusion layers, crosssectional area of metal lines, power dissipation density and switching speed will be presented at the Conference.



A 1. gate oxide breakdown

2. conductance between gate electrode and substrate

B 1. drain avalanche breakdown

2. effect of device temperature rise on V_T

C 1. modulation of channel length

2. short-channel effect due to scattering in device channel length

D 1. Power dissipation density

2. switching speed

Fig. 1 Diagram Illustrating Relationship among T_{ox}, V_{DD}, N_A and L.

References

1) B. Hoeneisen and C.A. Mead, Solid State Electronics, 15, p. 819 (1972)

2) B. Hoeneisen and C.A. Mead, Solid State Electronics, 15, p. 891 (1972)

3) R.H. Dennard et al., IEEE J. of Solid-State Circuits, SC-9, p. 256 (1974)

4) J.T. Wallmark, Electronic Engineering, 47, No. 564, p. 52 (1975)

5) R.W. Keyes, Proc. of IEEE, 63, p. 740 (1975)