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Since the implementation of the first planar transistor in 1959, the complexity of the circuits that can be realized on a single silicon chip has increased to the point where 100 kbit memory devices may be implemented, which corresponds to a doubling of chip complexity every year. Part of this evolution is due to technological advances. Refined photolithographic procedures have permitted the minimum feasible feature dimension to shrink to a few microns, and thereby have led to a corresponding increase in the number of circuits per unit area of silicon. In parallel, a continuously improving processing technology of the silicon wafer has reduced the number of defects per unit area that are introduced in each step. Thus, it has become possible to accept more complicated processing sequences and larger chip areas without reducing the overall manufacturing yields below commercially viable values. These two factors, chip size and feature density, however, can only account for a fraction of the actual growth in on-chip circuit complexity.

An equally large part of the observed advances has to be attributed to the ingenuity of the design engineers. Circuit designers have found ways to make more efficient use of the characteristics of semiconductor devices and thereby to reduce the number of devices that are required to perform a certain function. Layouts, too, have become more and more efficient. Contact windows, which use up area without providing any useful function from a signal-processing point of view, have been eliminated as much as possible. And similarly, the "useless" isolation area between adjacent devices has been minimized. At the same time device designers have developed structures which integrate individual devices in a much more efficient way and thus permit a significant device concentration. Ultimately, the individual devices may even lose their identity and merge to act as fully integrated functional blocks which are optimized to perform a particular task.

An example which clearly illustrates these trends is the evolution of the unit cell of random access semiconductor memories. While the circuit complexity was reduced from six transistors to a single one, the number of geometrical features necessary to implement the single transistor cell has been further reduced by using several levels of interconnection and by merging the transistor and the capacitor in the cell to a two-electrode charge-coupled readout structure. A corresponding evolution has lead from individual bipolar transistors

to the merged structures of integrated injection logic.

The trend in layout to minimize the number of separate geometrical features required for any one function has also led to such schemes as DMOS and VMOS transistors, where the length of the FET channel is defined by the difference in the depth of two subsequent diffusion processes or by the thickness of an epitaxial layer, rather than by a separate mask feature. Not only can this approach produce features smaller than the minimum photolithographic dimension, but also the accumulation of registration tolerances between subsequent mask levels can be eliminated.

In view of these developments of the last fifteen years, one can try to project the growth of integrated circuit complexity into the future. There is no indication that the two first mentioned growth factors, chip size and density, will slow down during the next five to ten years. Processing methods are still being refined, new techniques such as plasma etching and ion milling reach maturity and procedures are becoming automated thus reducing contamination or deterioration due to operator mishandling. Also, the minimum feature dimensions will continue to shrink for several more years. Powerful new photolithographical techniques using electron optics, scanned electron beams or X-ray will shrink the minimum features to the submicron range; features are still a long way from any fundamental physical limitations.

The factor that is hardest to predict is the course that ingenious designers will steer. It appears that we have come to a logical end of what appears now a reasonably straight-forward path of simplification, and it is difficult to imagine how a memory cell can be reduced to less than two features square. A conceivable way out of the apparent dead end may rely on a more efficient usage of the third dimension by stacking more features vertically and thereby further increasing on-chip function density.

In any case, integrated functional devices with a complexity in excess of what would correspond to 10^6 bits of memory or 10^5 logic gates can be expected within the next decade. By that time the major problem areas may well have shifted away from the fabrication to the testing of these complicated products.