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A-1-3 Stepped Electrode Transistor : SET

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A completely new structure of bipolar transistor was devised where high performance can be achieved without using precise photolithography and metalization techniques. The transistor is called Stepped Electrode Transistor or SET.

Figure 1 shows the structure of SET, in which the arsenic doped polycrystalline silicon which is processed to have a shape of inverse trapezoid is used as a part of the emitter electrode. The edge of the inverse trapezoid serves to form a shadow in making the base and emitter electrode through evaporation. The emitter electrode is separated from the base electrode electrically as the shaded area makes a gap between them. The characteristics of SET are compared with those of a conventional planar transistor in Table 1.

To fabricate SET, double layers of polycrystalline silicon of about 0.6μm thick are deposited on the base diffused layer through CVD process. The upper non-doped layer is of 0.2μm thick and the lower layer with 0.4μm thickness is highly doped with arsenic (1×10^{21}atoms/cm^3).A masked etch leaves inverse trapezoid polycrystalline silicon with overhanging sides on the roof top of the emitter electrode, because highly doped polycrystalline silicon is etched 10 times faster than non-doped one in the HF-HNO_3-H_2O system.

An unmasked ion-implantation process is used to selectively increase the susceptibility for etching of the unshadowed insulating layers (SiO_2+Si_3N_4),i.e.,the base contact and emitter contact windows. (Fig.2) The etching speed of the area implanted with boron ions (1×10^{15}/cm^2 at 40KeV) is 2 to 3 times faster than the unimplanted area in the buffered HF solution for SiO_2 film whereas 3 to 4 times faster in the boiled H_3PO_4 for Si_3N_4film.

Figure 3 shows a scanning electron micrography of SET. Figure 4 shows the frequency characteristic of $|S^e_{21}|$ and $|H^e_{21}|$, where cut off frequency of $|S^e_{21}|$ is 8.4GHz. This frequency is higher than that of the planar transistor by about 2GHz. The emitter area of this transistor is about 350μm^2.

Figure 5 shows the switching characteristics of integrated transistor in which rise time is 150psec. The emitter area is about 40μm^2.

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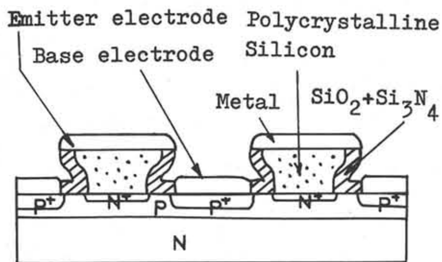

Fig.1 SET structure.

Items	Planar Transistor	SET
1. Number of photolithography processes that need precise alignment below 0.3μm.	3	0
2. Length between emitter diffused area and base contact.	1.5-2μm	less than 0.4μm
3. Mask alignment tolerance for making electrode.	about 0.2μm	2-3μm
4. Emitter diffused area width.	over 1μm	less than 0.5μm
5. Base-collector junction capacitance.	1	~0.5
6. Base resistance.	1	~0.5

Table 1. SET Features compared to the conventional same size planar transistor.

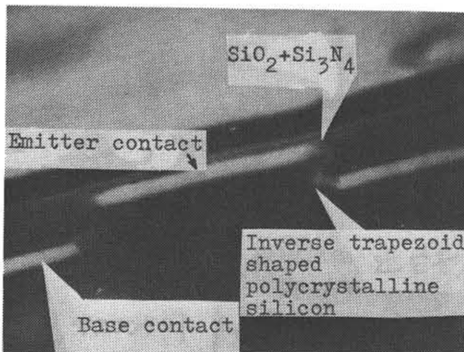

Fig.2 Cross-sectional view after a selective etching process. (scanning electron micrography)

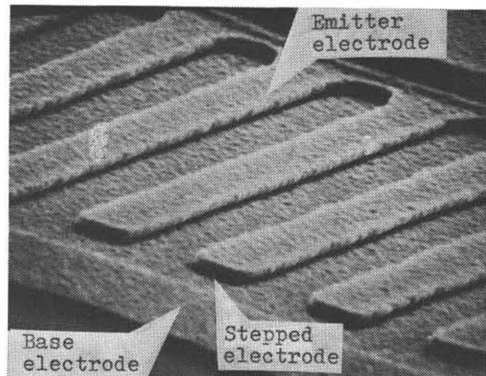

Fig.3 Scanning electron micrography of SET.

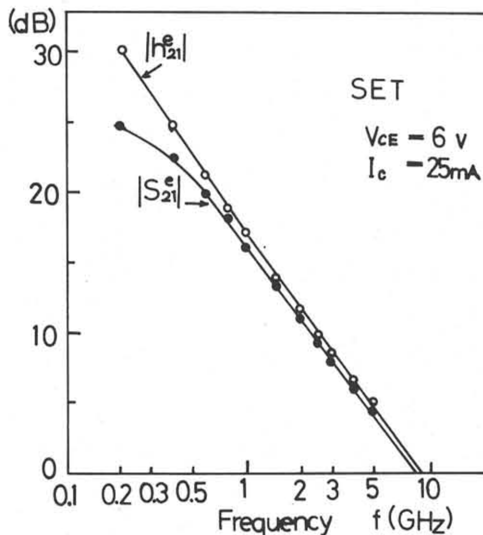

Fig.4 $|S^e_{21}|$, $|h^e_{21}|$ frequency characteristics.

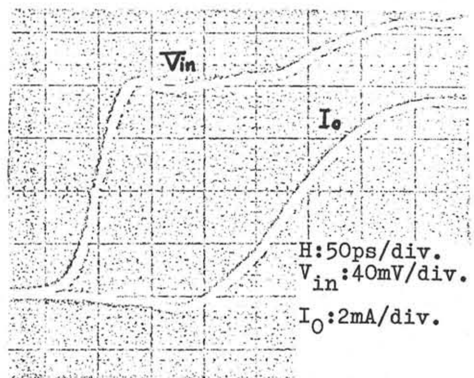

Fig.5 Switching characteristic of SET. (IC)