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(INVITED)

Vertical Injection Logic
-An improved form of Integrated Injection Logic-

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An advanced structure VIL(Vertical Injection Logic) has been developed for increasing a current gain and decreasing the minimum delay time in I^2L[1][2][3]. VIL uses a vertical pnp transistor in place of a lateral pnp transistor to get a uniformly narrow base width without degrading the electrical characteristics. Fig.1 indicates the both cross sections of conventional I^2L and VIL. In VIL, the injector is formed within the bottom n^+buried layer by the bottom injector p^+diffusion. The typical device parameters of I^2L and VIL are shown on Table 1. The value of α thus obtained was 0.3-0.5 for conventional I^2L and 0.6-0.9 for VIL. In Fig.2, the propagation delay time was plotted versus power dissipation. The experimental results show a minimum stage delay of 8.8 ns and a power-delay product of 0.07 pJ compared to 25 ns and 0.18 pJ for the usual I^2L.

The improvement of the power-delay product and the minimum delay time can be explained as follows. At low power ranges, higher α of VIL than that of I^2L results in the lower power-delay product. At high power levels, the minimum delay time is mainly determined by the hole storage in the epitaxial layer under the base region of the npn transistor as shown in Fig.3. Fig.3 shows the base current waveform which flows in the inverse direction after switching off the base driving. Total charges stored in the epitaxial region decreases with increasing χ which is the bottom injector area S_B ratio to the base area S_{BI}. Namely, the bottom p^+ injector is considered to act as a hole sink.

The capability of the very low power-delay product in the extrinsic region was applied to one chip wrist-watch and the low propagation delay time in the intrinsic region was used to the static RAM. Table 2 shows the electrical characteristics of analog watches for conventional I^2L, VIL and CMOS. It is expected that the same electrical performance with CMOS may be realized on one-half chip area. A static bipolar flip-flop memory of 1024 bits was realized by using this new structure. A microphotograph of the entire chip is shown in Fig.4. The address access time was measured to reveal a value of 400 ns at 10 mW power supply.

In summary, the new structure VIL was proposed and it's suitable application field was mentioned.

[1] K.Hart and A.Slob,IEEE J.Solid State Circuits,vol.SC-7(1972)346

[2] H.H.Berger and S.K.Wiedman,IEEE J.Solid State Circuits,vol.SC-7(1972)340

[3] T.Nakano et al., IEDM Technical Digest,Washington D.C.,(1975)555

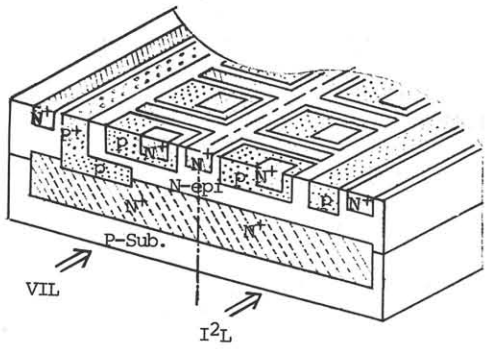

Fig.1 Schematic cross section of VIL and I^2L

Table 1 Typical device parameters of VIL and I^2L

	PNP		NPN	
	α	BVceo	β	BVceo
I^2L	0.3-0.5	30 V	5-16	5 V
VIL	0.6-0.9	30 V	4-13	5 V

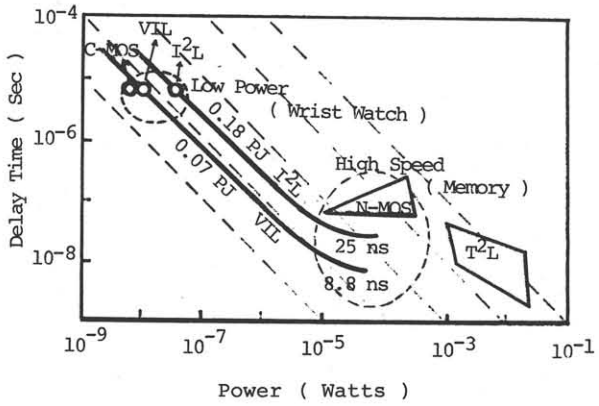

Fig.2 Power-delay curves measured from inverter chains

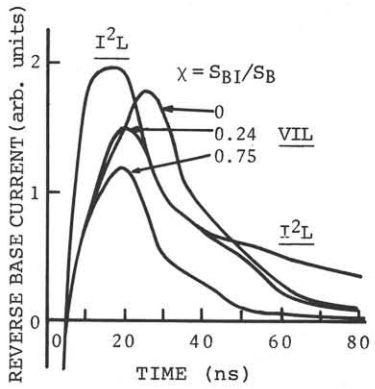

Fig.3 Base current waveform which flows inverse direction after swiching off base driving.

Table 2 Comparison of analog-wristwatch IC properties

SUPPLY VOLTAGE 1.5 V

	I^2L	VIL	CMOS	VIL (EXPECTED)
OSCILLATOR/DIVIDER CURRENT (μA)	12.4	4.0	1.5	1.4
MOTOR DRIVE CURRENT (μA) (LOAD 3.5 kΩ)	370	400	400	420
CHIP SIZE (mm^2)	4.8	4.8	4.0	2.3

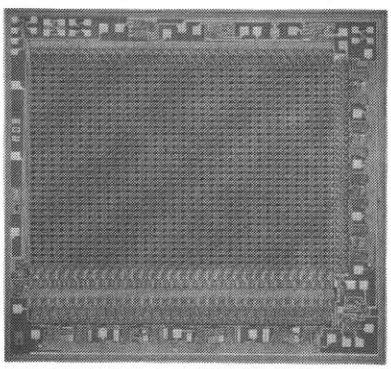

Fig.4 Microphotograph of 1024 bits RAM. Entire chip is 4.4 X 4.0 mm^2.