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Phosphorous Buried Emitter I^2L for High-voltage Operating Circuits

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Phosphorous buried emitter I^2L has realized co-operation of I^2L circuits and high-voltage resistive bipolar circuits in one chip.

One of the most attractive features of I^2L is the capability of making monolithic LSI's with conventional bipolar devices. However, breakdown voltages of bipolar devices have been limited to less than 10 volts, because I^2L requires high inverse current gain and, as a result, thin epitaxial layers. Consequently, application of I^2L has been confined to low-voltage operating fields such as watches[1] and microprocessors.[2]

This paper will describe an approach in realizing I^2L circuits in conjunction with high-voltage resistive bipolar circuits which have 22 volts in BV_{CEO}. In the structure discussed, shown in Fig.1, phosphorous buried N^+ **layers** were introduced to obtain highly up-diffused buried emitters and resulting thin residual epitaxial layers for I^2L. Antimonide buried N^+ layers were used for conventional bipolar circuits. A photomicrograph for a cross sectional view of the device is shown in Fig.2. The device was made with the usual planar technologies without any special technique that affects yield problems. Only one diffusion process is added to the standard process. Phosphorous buried layers are well up-diffused to reach base regions compared to antimonide buried layers as shown in Fig.2.

The current dependence of inverse current gain β_u is shown in Fig.3. β_u is increased 2.5 times over that of conventional I^2L, by applying phosphorous buried emitters as shown in the figure. The operation parameters of bipolar transistors and I^2L devices fabricated on a same chip are summarized in Table 1. A thick epitaxial layer caused high breakdown voltages, about 22 volts in BV_{CEO} and 58 volts in BV_{CBO}, for bipolar transistors. As a result, only phosphorous buried emitter I^2L could operate successfully due to its increased inverse current gain properties. The 5-stage ring oscillator measurement showed 0.3 pJ/stage in power delay product and 20 nS in minimum delay time.

In summary, it has been established that I^2L circuits can operate even in a high-voltage operating LSI chip through the discussed approach. This fact should considerably expand I^2L's field of application.

1) P.A.Tucci and L.K.Russel : ISSCC 76 7.1 (Feb. '76) et.al.
2) R.L.Horton, J.Englade and G.McGee : Electronics, Feb.6,'75, PP83-90

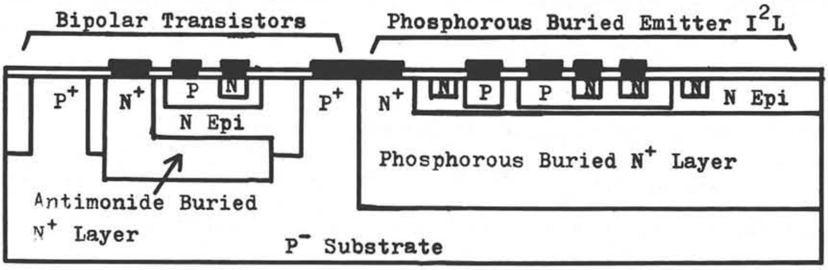

Fig.1 Schematic cross section of the phosphorous buried emitter I^2L

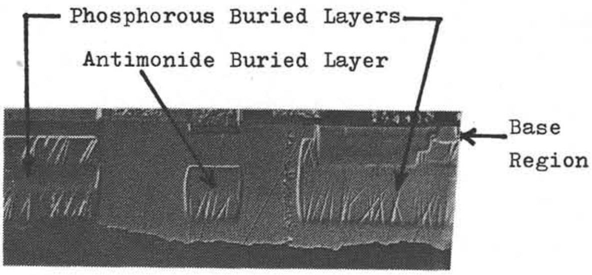

Fig.2 Photomicrograph of 5°-angle lapping of the fabricated device.

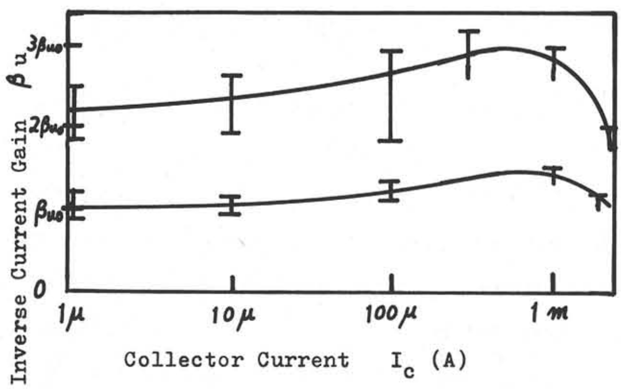

Fig.3 Current dependence of inverse current gain β_u.

Upper: Phosphorous Buried Emitter I^2L.
Lower: Conventional I^2L.

Table 1 Operation Parameters of bipolar transistors and I^2L devices.

NPN Transistors	
Gain β_d	120
BV_{CBO}	58 (V)
BV_{CEO}	22 (V)
BV_{EBO}	7 (V)
Phosphorous Buried Emitter I^2L	
Inverse Gain β_u (two-collector)	5
Normal Gain β_d	150
BV_{CBO}	7 (V)
I^2L Operation	○
$P \cdot t_{pd}$/stage	0.3 (pJ)
$t_{pd\ min}$	20 (nS)
Conventional I^2L	
Inverse Gain β_u (two-collector)	2
Normal Gain β_d	120
BV_{CBO}	7 (V)
I^2L Operation	×
$P \cdot t_{pd}$/stage	×
$t_{pd\ min}$	×