A-2-6 Static Induction Logic — A Simple Structure With Very Low Switching Energy and Very High Packing Density

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I. Introduction

The current trend in integrated logic circuit design is towards the reduction of both the delay time and the supply power. At present, the I^2L structure [1,2] offers the lowest switching energy. Further reduction of this energy can be achieved in the VIL structure[3] in which the supply power efficiency has been increased due to the increased injector current gain. However, the VIL structure requires eight masking steps. On the other hand, the Substrate-Fed-Logic[4] provides higher packing densities. The new transistor-type introduced here allows further reduction in the power-delay product.

II. The new type of transistor

The structure of this new type of transistor is shown in Fig.1. The channel impurity concentration is low enough so that even without any bias applied, the channel is depleted of carriers due to the built-in potential on the pn^- interface. For negative and upto small positive gate potentials, this transistor operates as a Static Induction Transistor which was introduced by J.Nishizawa et al.[5]. At still higher positive gate potentials, both holes from the gate and electrons from the source are injected into the channel region. Because of the built-in field at the n^+n^- interface only the electrons can travel from the source to the drain, while the holes injected from the gate (for small drain voltages) create a static change in the channel region. The gate current (for positive bias on the gate) is caused mainly by the hole-electron recombination in the channel region. Direct injection of carriers both from the source to the gate (electrons) and from the gate to the source (holes) is comparitively small because of the presence of the built-in field. In a logic circuit this transistor operates in both of the modes — the SIT mode for the high output-voltage level and the gate injection mode for the low output-voltage level.

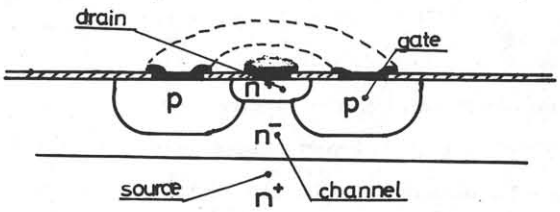

Fig.1

III. Low delay-power product

The delay-power product for the I^2L structure is equal to

$$\tau_d P = \frac{I_{su}}{I_i} V_{su} V_{sw} C_t \quad (1)$$

where V_{su}, I_{su}: supply voltage and current,

V_{sw}: voltage-swing between the two logical levels,

C_t: total capacitance $C_t = C_{eb} + 2C_{cb}$ in the I^2L case, or $C_t = C_{sg} + 2C_{dg}$ in the case of the structure presented here.

In VIL structure the I_{su}/I_i ratio has been decreased by a factor of two. More significant reduction in the

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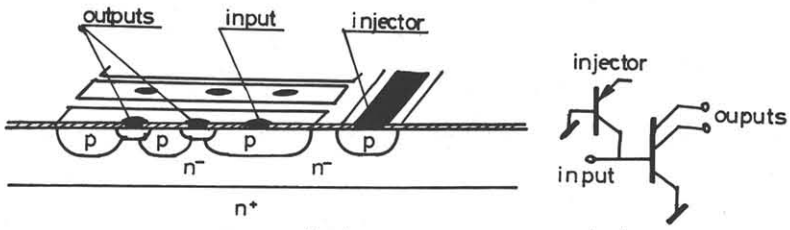
value of expresion[1]) is caused in case of the logic structure shown in Fig.2 by the fact that the effective impurity concentration both at the source-gate and at the drain-gate junctions is about 2-orders of magnitude lower than in the I^2L case. Hence for the same circuit size the total capacitance is about 10 times lower. This makes the presented logic have a very small delay-power product, even lower than 0.01pJ.

IV. 3-mask technoloty

As in the usual cases the logic structure presented in Fig.2 needs only 4 masking operations (p-diffusions, n-diffusion, contact holes, metallization). However because of this specific structure, wherein the entire wafer area can consist of either p-type diffused or n-type diffused regions only, it is possible to use only one mask for both p-type and n-type diffusions. One of the known technological methods can be used for this purpose, e.g. boron doped SiO_2, or Si_3N_4 masking. This reduction in the number of masking operations required permits further miniaturization of the devices.



(a) (b)

Fig.2

V. High packing density

In the I^2L structure all gates must be isolated by a deeply diffused n-layer to prevent lateral injection between gates. This is especially important because in the I^2L structure the npn transistor current gain is low (inversed mode) which results in a very low noise margin. Thus, if we do not use n-type isolation-diffusion in the I^2L, the circuit may not operate at all. In the case of the proposed structure, however the lateral diffusion between gates does not affect the circuit operation (no gate current 0 input level and very small gate current for 1 input level). On the contrary, this lateral injection between gates decreases the delay time, since the effective supply current is higher due to this effect making an n-type isolation diffusion layer is unnecessary. This permits very high packing densities upto 1000 two-input gates per mm^2. In the Fig.3 a structure with vertical injectors is shown. This modification allows for further increase in the packing density, upto about 2000 gates per mm^2. Therefore the packing density is practically limited by the metal interconection between gates.

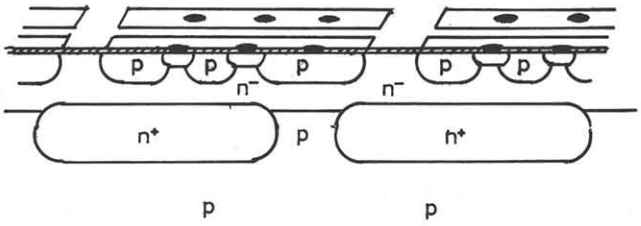


Fig.3

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