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Future Trend of Static Induction Transistor and Its Application for Integrated Circuits

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Static Induction Transistor[1] has already realized in the form of low distortion audio transistor, of high power transistor of about 2KW d.c. with the α-cut off frequency of about 7MHz, and of EHF transistor of about 3.7W a.c. at 2GHz. And, also, the applications into the thyristor structure and into the integrated circuit seems promissing.

The similar structure of pararell electrodes with multichannel which is analogous to the vacuum tube triode, exactly light house tube triode, was proposed by Watanabe et al.[2] in 1950 and the space charge conduction laws in diode lead[3] also in 1950, both followed by W.Shockley[4] in 1952 of cylindrical structure[5], however, any person has not yet succeeded to realize triode character reproducibly. Only Zuleeg[6] succeeded to realize similar character which based on punch through in bipolar transistor which was unexpectedly realized by the surface diffusion in the preparation of analogous transistor to vacuum tube triode, which was also followed by Teszner[7]. Moreover, their "analog transistors" were published to show space charge conduction law. The SIT which is exactly analogous structure to vacuum tube triode shows exponential character followed by the effect of negative feed back and the series resistance[1], however, restricted to keep the series channel resistance as small as $g_m \cdot r_s < 1$.

Then we now have three types of transistors, the first one is usual bipolar (BPT), the second is, so have called, FET and the third is this SIT, which shows FET like characteristic about gate and BPT like injection characteristics about drain current. Therefore, the SIT summarized best point from both transistors ; BPT & FET. Moreover, it has been clarified that the magnitude of the channel resistance divide the characteristics into FET and SIT[1]. Then the SIT corresponds to the extreme case of the FET with very small channel resistance, which is enough to expect the small time constant between gate and source which is equivalent to the fact that the cut-off frequency is the highest and the noise is the least compared to those of the FET & the BPT, as well as high transconductance and low output impedance caused from the small negative feed-back action.

About the structure of the gate, as same as FET, it can be very very highly doped, which is restricted not to reduce the injection ratio γ in the case of the BPT. Therefore the gate series resistance, corresponding to the base resistance in BPT, can be very low which permit to prepare very large area and very long length.

In SIT and FET, the MOS structure can be extremely low resistance along the gate, moreover, multi-channel structure make it easier to prepare large area devices, cooporating with overwhelmingly small capacitance between gate and channel compared with that between base and emitter in BPT.

As a whole, the figure of merit is nearly the same about the item of between gate and drain, and about the structure of the gate, the FET & SIT are much superior compared with BPT. And about the structure between gate & source (base & emitter), SIT is extremely superior compared with BPT and better even with FET.

Then the SIT is expected to be the most powerful devices even in EHF region. Small gate (base) resistance and high input impedance makes possible to realize large area devices. Figure 1 shows the top-viewed pattern of the actual SIT, which can generate several Watts at 2GHz. Source is n-type, gate is p-type and both are diffused from the surface with mask technology.

Another interesting feature of SIT is that the flowing current from source to drain is squeezed by the backward bias of gate electrodes, therefore, the area ratio of source to that of drain can be small, which should be larger than 1 in usual BPT.

This is also very convenient properties for high frequency application, because the stray capacitance can be decreased by the introduction of mesa structure for the drain. And moreover, the integration of SIT into integrated circuit seems also very convenient by the same reason, which helps to fasten the operating speed, in addition to the very small time constant of operation which depends on the products $C_{gs} \cdot r_s$ (where r_s represents series channel resistance).

Energy of operation of SIT logic (SIL), including MOSSIL, is expected to be very small, because the point of operation is not after the saturation but only over noise level. Moreover, the differential resistance at the operating point is low which is helpful to have high speed, in the same time it has disadvantages not to show saturated mode of operation. However, it can be calculated $W \cdot \Delta t$ is 6×10^{-3} times smaller compared with bipolar logic when it is assumed constract I^2L.

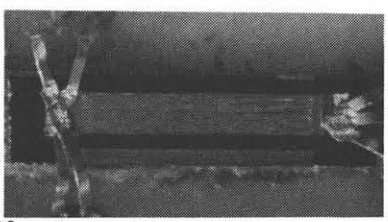

Fig. 1

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