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DSA MOS transistor and its Integrated Circuit

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In 1969, superiority of the MOS transistor in the frequency region as implied in Einstein's relation was demonstrated by experimental devices(1)(2) with a short channel made by double diffusion technology and with reduced feed back capacitance by V-shaped groove structure(fig.1(a)) or by stepped gate oxide(fig.1(b)). Since then, many researchers have developed various version of transistors and IC's as shown in table 1.

As one of characteristic features confirmed by the authors in table 1, DSA MOS transistors have a smaller input capacitance for a given current driving capability and are capable to realize faster speed in LSI than other MOS devices, but it is still useful to reduce gate electrode length or source to drain distance L_{DS} for high speed with low power dissipation. In conventional MOS transistors, reduction of channel length causes uncontrolability of device parameters such as V_{th}. V_{th} of conventional MOS transistor changes appreciablly for the L_{DS} of 4 μ as shown in fig.2, but V_{th} of a DSA MOS transistor stays nearly constant down to L_{DS} of 1 μ, resulting loose photoetching tolerance to realize designed device parameters. DSA MOS transistors with source to drain distance of the order of 1000 Å will be further realized by applying modified scaling concept with advantage of using thicker gate oxide than that of conventional MOS transistors.

In near future, dynamic and static 4 K DSA MOS RAMS will be announced with access time of 50 ns or faster. DSA MOS transistors also have no obstacle to realize a high speed microprocessor with cycle time of the order of 100 ns and also a power MOS device operating at 10 GH_z by a present day fabrication technology.

fig.1 Various types of DSA MOST's

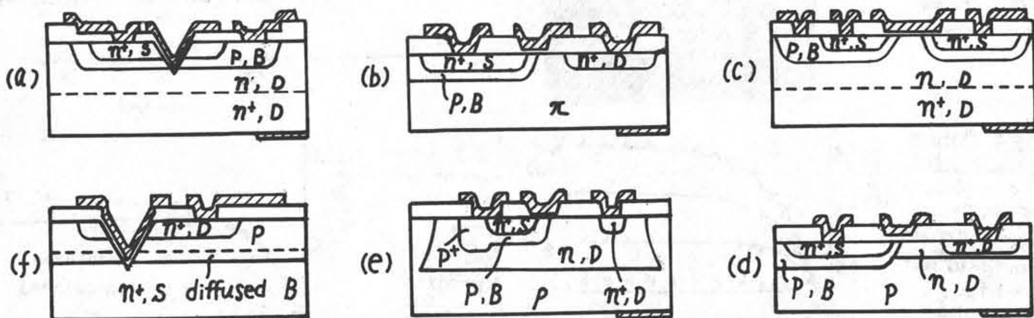

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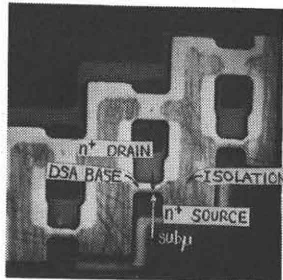
Table I

Performance or Obtained results	Author, Journal or Conference, Year
Proposal of a DSA MOST as a high speed sub-μ channel device with high drain avalanche break down voltage and no punch through effect. experimental devices (fig.1(a),1(c)); f_1=6.8GH_z	[1] Y. Tarui et al. 1st this conference 4-1, 1969
π planar type with stepped gate oxide(fig.1(b)); 11 dB at 1GH_z on resistance design by E/D concept. DSA lateral bipolar transistor.	[2] Y. Tarui et al. 4th Microelectronics Congress in Munch, 1970
DSA-ED-MOS-IC; t_p=1.2ns & t_p·p=2.4pJ or t_p·p=0.24pJ	[3] Y. Tarui et al. 2nd this conference 6-2 and IEDM 17.2, 1970
D MOST fig.1(d); f_{max}=10GH_z, NF=4dB(1GH_z), or BV_{DS}=300V	[4] H.J.Sigg et al; IEDM Late News 12.7, 1970, Electronics Feb.15, 1971 and IE^3 Trans., ED-19, 1, 1972
computor analysis of output characteristics in triode region V_{th} controlability (BV_{DS}=250 V).	[5] Y. Tarui et al; Joint National Convention of 4 Institutes of Japan, 1970 [6] H.C.Lin et al; IE^3 Trans., ED-20, 3, 1973 [7] M.D.Poche et al; IE^3 Trans., ED-21, 12, 1974
D MOS(fig.1(e)) 200 volt multiplexer with level shifter. it's complementary version.	[8] J.D.Plummer et al; ISSCC THPM 14.2, 1974 [9] J.D.Plummer et al; ISSCC FAM 17.4, 1976
V MOS(fig.1(f)), high density, high speed, TTL compatible, t_p=2~3 ns. V MOS 16 K ROM.	[10]T.J.Rodgers et al; ISSCC THAM 10.4, 1974 [11]T.J.Rodgers et al; ISSCC WPM 6.4, 1976
gm vs. V_G by E/D concept including saturation velocity effect.	[12]T.J.Rodgers et al; ISSCC THPM 11.4, 1975
DSA-ED-MOS-LSI, 4 bit ALU; t_p=2.9ns, t_p·p=2pJ, Ring Oscillator; t_p=0.65ns, t_p·p=0.1pJ	[13]K. Ohta et al; ISSCC THPM 11.5, 1975
computor analysis of out put characteristics over full region(fig.3)	[14]T. Sekigawa et al; Trans. IECE of Japan, 58-C, 9, 1975
V_{SUB} dependence of V_{th} (fig.4)	[15]T. Sekigawa et al; National Conv. of IECE of Japan, 351, 1976
dynamic 1 K RAM; access time=50 ns	[16]K. Shimotoru et al; National Conv. of IECE of Japan, 372, 1976
SOS DSA MOST; 10 times higher gm than conventional device and reduced kink effect.	[17]Y. Sakai et al; Technical report of IECEJ, SSD 75-3, 1975
V_{th} controlablity by double ion implantaion	[18]I. Ohkura et al; this conference A-3-3,1976
750 V drain breakdown voltage	[19]T. Biwa et al; 23rd. joint national convention of Japanese institutes related to applied physics, 27a-N-11, 1976

Microphotograph of surface stained DSA ED MOS IC shows self-aligned subμ base, in the surface of which subμ channel is induced.



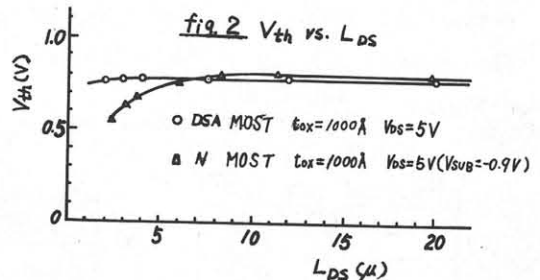


fig.3 Output characteristics of a π planar DSA MOST.
$N_{BS}=8\times10^{16}cm^{-3}$
$N_{BD}=2\times10^{15}cm^{-3}$
$L=1.1\mu$
$t_{ox}=1300Å$
$L_{DS}=3.5\mu$

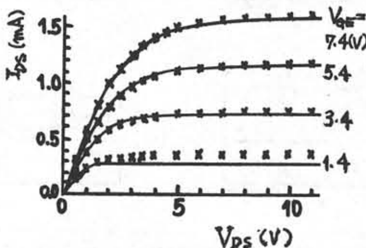


fig.4 Increment of Vth vs. substrate bias, VSUB.
$N_{BS}=2.5\times10^{16}$
$N_{BD}=1\times10^{14}$ (cm^{-3})
$L=2.7\mu$
$t_{ox}=890Å$
$L_{DS}\approx100\mu$