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A-3-4 Analytical Techniques for the Design of DMOS Transistors*

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Several promising applications of double-diffused MOS transistors in integrated circuits have been reported,[1,2] and interest in these structures seems certain to increase. The DMOS transistor has some major advantages such as high transconductance, high speed and high voltage operation that are obtained without the necessity of extraordinary processing and mask tolerances.

For an accurate analysis of a DMOS transistor, it is necessary to consider a number of second-order effects. Previous models[3-6] have used varying levels of approximate analysis, but their accuracies have not been entirely satisfactory.

This paper describes a new analysis program for DMOS transistors that features an accurate forecast of the current-voltage behavior in various DMOS structures. The model of a typical asymmetrical DMOS transistor is shown in Fig. 1. The model basically consists of (1) p-type channel region, (2) n-type drift region, and (3) drain region. The analysis is basically one-dimensional in regions (1) and (2), where accurate values of the surface potential is obtained numerically first, and the corresponding induced electron charge Q_n is then calculated at each point. The charge is integrated so that the current continuity condition for both drift and diffusion components is satisfied in the source-to-drain direction. In the drain region, it is assumed that the charge is injected from the channel and that the shape of the space-charge region is triangular. Thus, Poisson's equation including a mobile charge is integrated in this region. The analysis takes account of the dependence of electron mobility upon gate and drain fields and upon doping density at each point.

Figure 2 illustrates several structures to be analyzed. These include standard DMOS transistors having asymmetrical doping profiles and the DMOS transistor with symmetrical doping profiles. The main applications of the symmetrical DMOS transistors are dynamic memories where bi-lateral switching action is needed. A simple CMOS process utilizing the symmetrical DMOS transistor has also been reported by the authors.[7]

Figure 3 is a comparison of the theory with experiment for a p-n type asymmetrical DMOS transistor. It is seen that the agreement in non-saturation region is

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region is excellent. The deviation in saturation region arises from the form of the velocity saturation equation used.

A comparison of the surface mobilities and quasi-Fermi potentials along the channel is shown in Fig. 4 for: (1) a standard MOS transistor, (2) a p-n type asymmetrical DMOS transistor, and (3) a p-p type symmetrical DMOS transistor. Through this comparison, it is found that the field is greatest at the source end of the channel in DMOS transistors, and the saturation drain voltage depends on the doping type and level near the drain diffusion. It is also determined that the p-n type device has the highest saturation drain current. The detailed discussion will be made on the point (1) comparison of the several DMOS structures, (2) the effect of shrinking the gate length down to approximately one micron in a DMOS transistor.

The computation time for the set of curves, for example those shown in Fig. 3, is 125 sec. with a CDC-6400 computer. This is much faster than two-dimensional analysis. Thus, the present analysis provides an effective design tool for optimizing device structure, channel lengths and doping profiles in DMOS transistors.

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