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Nonvolatile Semiconductor Memory

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Semiconductor memory with nonvolatility has been widely studied with much interest, and several attempts have been tried to explore feasibility of an erasable read only memory (EROM), a nonvolatile read write memory (NVRWM), optical data storage, content addressable memory, discrete analog signal processing etc. Physical mechanism of nonvolatile data storage in various kinds of device structures has been also extensively studied, which has strongly stimulated rather basic research on the emission, injection and transport phenomena of electronic charges in the silicon-insulator systems. The purpose of this paper is to describe the recent progress in the nonvolatile memory devices and to discuss various features of these devices. Although there might be many interesting subjects in the field of amorphous memory, we would restrict our scope within the silicon technology.

There are two typical device structures; (a) a metal-insulator-oxide-silicon (MIOS) structure and (b) a floating gate structure, both of which are utlizing the change in the threshold voltage of MOS transistor due to increase/decrease of charges in the gate insulator region to store the data with nonvolatility.

MIOS devices

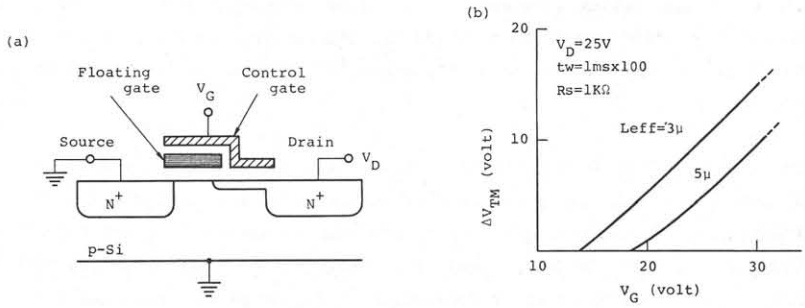
Nonvolatility comes from the electronic charges which are being captured at the traps in the insulator,(I), unless otherwise being released by the external voltage applied to the gate. Since the writing/erasing speed strongly depends upon the mechanism of charge transfer through the oxide layer, most of the MIOS devices have tunnelable oxide of approximately 20 Å thick which results in faster speed compared to other mechanisms. The speed is again accelerated by introducing excess traps in the insulator, which has been achieved by the modified structures of metal-insulator-metal-oxide-silicon[1] and metal-insulator-silicon-oxide-silicon[2]. The insulator is usually silicon nitride (MNOS) and sometimes aluminum oxide (MAOS). The writing/erasing of an information is by the direct tunneling of either electrons or holes through the ultra thin oxide in most of the cases, but a combination of the direct tunneling and the avalanche injection was tried to make single polarity writing.[3] Typical writing/erasing speed is in the order of 10^{-3} to 10^{-5}sec at 30 volts, and is much faster in case of the modified structures. As the EROM or the electrically alterable ROM (EAROM) MIOS gives rise to satisfactory characteristics, and 256-, 1024- and 2048-bit LSI memory have been developed already. On the other hand significant problem has been pointed out when one expects to use the MIOS device as an NVRWM, which is the performance degradation during writing/erasing cycles. After 10^{5-8}cycles, the threshold voltages for both "1" and "0" levels start changing and the retentivity also starts degrading, and thus the NVRWM has been difficult to be practically realized. The only approach to solve the problem is to utilize the MIOS memory to back up a conventional volatile memory, where the MIOS is operated only when power shortage occurs and the endurance of more than 10^{5-8} cycles would not be required any more. A 256-bit NVRWM has been developed by this approach.[4] The other interesting combination of MIOS with CCD has been proposed and will be a candidate for a nonvolatile memory with very high bit density[5]. As far as the physical mechanism is concerned, there still remain many unrevealed aspects even in the characterization of traps, and some of them essentially require better understanding of the silicon-silicon dioxide system.

Floating gate devices

In the structural point of view of the floating gate EROM transistors, there are two types: a floating gate structure (FAMOS)[6] and a stacked gate structure (SAMOS)[7]. The hot carrier injection type EROM's are divided into two groups in terms of programming method, one is avalanche injection and the other is non-avalanche injection.[8] The former uses electron injection from the avalanche plasma induced at the drain junction, and the latter uses the injection of hot electrons accelerated during transit in the channel or the injection of electrons by bulk p-n junction (ATMOS)[9].

In the case of the avalanche injection, rather high voltage is required to program the memory. On the other hand, the hot carrier injection is more desirable for memory application because of possibility of reducing the programming voltage. The channel accelerated injection method was proposed by Dill et al.[10] for the MNOS structure device.

In Fig.1 is shown the relationship between the control gate voltage, V_G, and the threshold voltage shift, ΔV_{TM}, in the channel injection type MOS erasable (CHIME) memory transistor. It is clear that the control gate voltage is effective to control ΔV_{TM} and the effective channel length, L_{eff}, has large influence on the generation of hot electrons. Though the ease in the hot electron generation means the possibility of poor memory retention, it has been revealed that the transistors having the effective channel length of longer than 3μm is reliable enough for PROM applications.



Structure of memory transistor

Writing Characteristics

Fig.1 CHIME memory transistor

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