Digest of Tech. Papers The 8th Conf. (1976 International) on Solid State Devices, Tokyo

A-3-8

New Two-Terminal C-MNOS Memory Cells

Susumu Koike, Gota Kano, Akio Kashiwakura, Ginjiro Kambara, and Iwao Teramoto
Research Laboratory, Matsushita Electronics Corporation
Takatsuki, Osaka, Japan

A new two-terminal nonvolatile memory cell is proposed, in which an n-channel MNOS transistor is functionally coupled with a p-channel depletion-mode MOS transistor as shown in Fig. 1. The operation principle of the cell is basically relying upon the Λ (lambda)-shape I-V curve of the complementary FET circuit.[1), 2)]

Principal advantages of the present cell array over the previously reported MNOS PROM's are as follows.

1) Since the two-terminal cells are of high impedance during writing and erasing processes, a simple diode-matrix works well as an integrated memory device. This advantage greatly reduces the device geometry and simplifies the peripheral circuit.
2) The diode-matrix can be operated with a unipolar power source without any isolation among the cells involved.
3) A selective writing/erasing operation is also possible in this simple diode-matrix so that the array can be used in a RAM-mode.

The present paper describes the structure and the operation of the proposed memory cell, together with experimental results on a 4x4 diode matrix array.

Figure 2 schematically shows a cross-sectional view of the two-terminal unit cell. A "0" memory, as shown in Fig. 3 (a), is stored in the cell unless a bias is applied to the two external terminals. To write "1", a negative pulse is applied to the T_1 terminal with respect to the T_2 terminal, transporting change carriers to the gate insulator of the MNOS FET from the substrate (p-well in Fig. 2). A Λ-shape I-V characteristic, as shown in Fig. 3 (b), is then stored and read out between the negatively biased terminals, because both FET's in the cell are now operating in a depletion-mode. For erasing the "1" memory, a negative pulse is applied to the T_2 terminal with respect to the T_1 terminal for transport

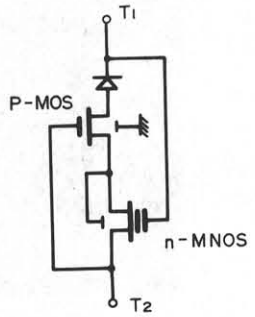

Fig. 1

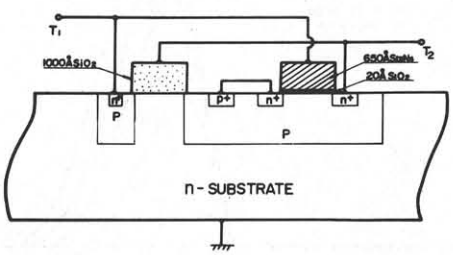

Fig. 2

of the stored carriers back to the substrate. It is to be noted that a unipolar source is used throughout these operations.

The same operation procedure is also applied to a modified cell structure[3], where the p-channel MOS FET in Fig. 1 is replaced with a p-channel MNOS FET.

The basic operation of the proposed cells has been examined using a 4x4 diode-matrix array. The experimental result on a ROM-mode operation has shown that the array successfully covers the Electrically Alterable PROM (EAPROM) application in such a simple manner as conventional fuse-type diode-matrix PROM's. In addition, the present cell-matrix can be used in a RAM-mode under unipolar pulses with no aid of isolation among the cells. As shown in Fig. 4, the writing or erasing of a memory in any one of cells is selectively achieved because every cell is maintained at high impedance regardless of the stored information.

Another interesting point to be noted is that the Λ-shape of negative resistance in the I-V characteristic curve changes with the height as well as the width of the writing pulse as shown in Fig. 5. This fact may be attractive to applications to analog memory devices.

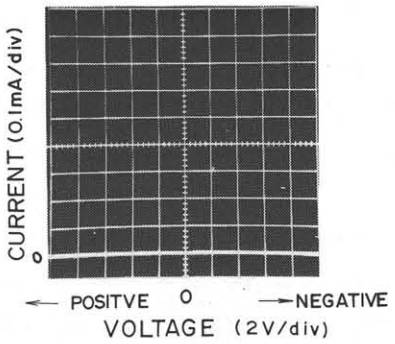

Fig. 3 (a)

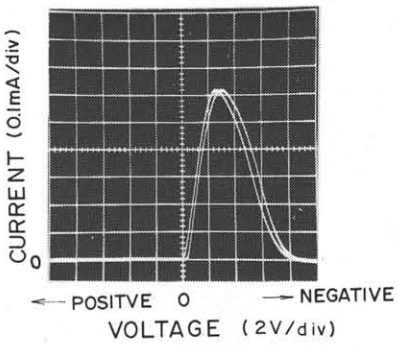

Fig. 3 (b)

Note: 1) G. Kano et al.: IEEE Trans. Vol. ED-21, pp.448, 1974.

2) H. Takagi et al.: IEEE Trans. Solid-State Circuits Vol. SC-10, No.6, pp.509, 1975

3) S. Koike et al.: Submitted to IEEE Trans. Electron Device.

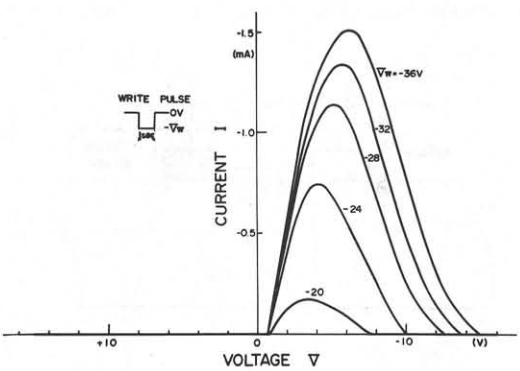

Fig. 5

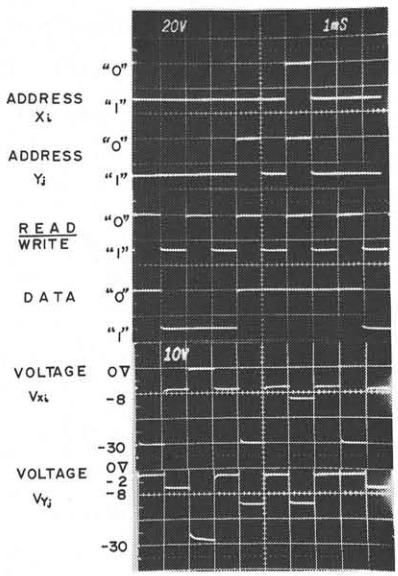

Fig. 4