

A-3-9

Studies of Localized Charge Injection in Surface Avalanched PN Junctions

R. Amantea* and R. S. Muller

Department of Electrical Engineering and Computer Sciences
and the Electronics Research Laboratory
University of California, Berkeley, California 94720

Charge injection into silicon oxide owing to surface avalanche is assuming mounting significance for device design and performance. Many of the general features of this phenomenon have been determined through earlier research. However, with the advent of short-channel MOS transistors, and as a result of the application of avalanche charge injection to new devices, more precise information about avalanche injection into oxides is needed. A new gated avalanche pn junction triode has been designed to obtain this information. This experimental device contains a unique split gate which permits the experimental determination of the centroid of the injected electron flux into the oxide. Because the injected currents are very small and the environment is noisy, special care must be taken to measure the currents accurately. The problem of accuracy is further accentuated by the influence of an offset voltage between the split gates on the bias of the avalanching junction below them. The construction of a special measuring circuit which yields reliable measurements despite these obstacles is described. Thus far, experiments with these triode structures have been confined to heavily doped p-regions forming junctions to lightly doped n-material. Measurements on these devices show that the centroid of the avalanching region undergoes a transient displacement away from the center toward the p-side of the

* RCA David-Sarnoff Fellow

Research sponsored by the U.S. Army Research Office Grant DAHCO4-75-G0108.

junction and then returns slowly to the center. Theory has been developed which relates this behavior to the trapping of electrons in the oxide. The new structure is therefore useful in ascertaining the electron trapping properties of the oxide as well as in developing further understanding of the nature of surface avalanche in the silicon. Further experiments with pn junctions doped in the opposite sense (lightly doped p-on heavily doped n-silicon) and with devices formed on silicon of various surface orientations are described.