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64 Stage BCD Analog Memory with Differential  
Integrated Clock Pulse Generator

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Charge transfer devices are on the verge of being put use in a number of analog signal processing systems such as TV ghost cancellors, video time base error correctors and so on. The performance of the devices, however, is severely limited by interference due to higher harmonic frequency components radiated from external clock pulse generators and output voltage fluctuation in varying the clock pulse frequency. Because unbalanced crosstalking and/or ringing of external clock pulses modulate the channel potential of the device, the conventional differential array configuration is not a solution to these problems.

(1)(2)  
Figure 1 shows the microphotograph of a 64 stage BCD(Bulk Charge-transfer Device) with a new differential integrated clock pulse generator that has been developed to eliminate these problems. Fig.2 shows the schematic layout diagram of the device. The key to the design is the method of laying out the peripheral circuits. As shown in Fig.1 and 2, two clock pulse circuits are laid out at the upper and lower parts symmetrically. These circuits drive the two separate BCD arrays.

(3)  
The features of this built-in differential pulse generator are as follows;

- (1) There is no cross point between the pulse lines, which eliminates crosstalking and ringing of the pulses. Fig.3 shows the pulse wave forms of the differential integrated pulse generator as compared with the ones of the conventional external circuit.
- (2) The built-in clock pulses can symmetrically fix the channel potential of the two arrays substantially decreasing voltage fluctuation and radiated noise.
- (3) Temperature balance along the two arrays is quite well because the two arrays accept the same thermal influence from the two pulse circuits that dissipate the equal power.

The BCDs with the peripheral circuits were fabricated by n-channel double poly-silicon gate technology. Another feature in process is the introduction of double implantation of P<sup>+</sup> and B<sup>+</sup> under transfer gates to make the potential gradient in the channel. The device runs from 4 kHz to 28 MHz with a wide range of output signal bandwidth. A dynamic range of 1.5 volts was obtained and the matching of the voltage transfer characteristics of the two arrays is as shown in Fig.4, resulting <sup>that</sup> differential output fluctuation of the two arrays was observed less than 52 dB in the range of below 15 MHz, that is, 23 dB improvement. In Fig.5, charge transfer characteristics show the total loss of less than 10% and the good matching of the two arrays, as well. This new BCD analog memory requires only one TTL level master pulse and two power supplies, which can save some 60% of peripheral components.

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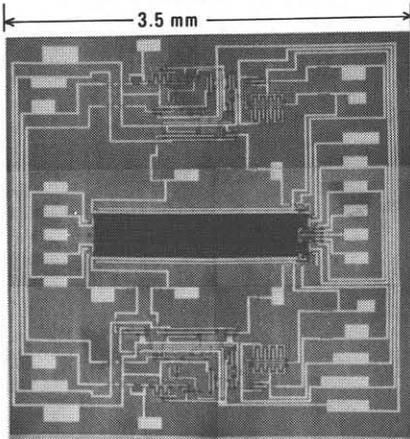


Fig.1 Microphotograph of 64 Stage BCD Analog Memory

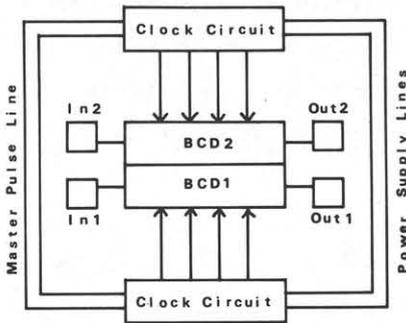


Fig.2 Layout of BCD Analog Memory and Differential Pulse Circuits

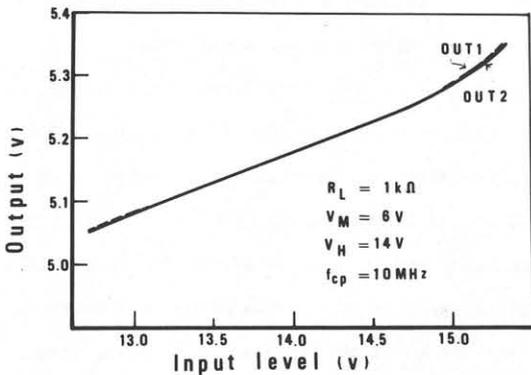


Fig.4 DC Voltage Transfer Characteristics

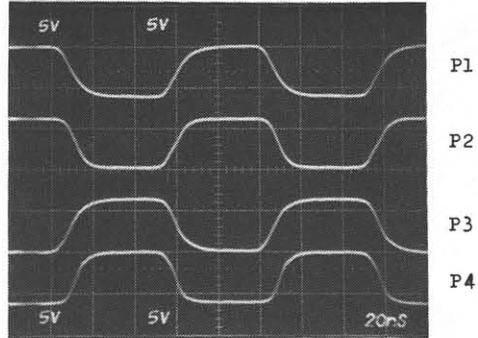


Fig.3(a) Clock Pulses of Integrated Circuits

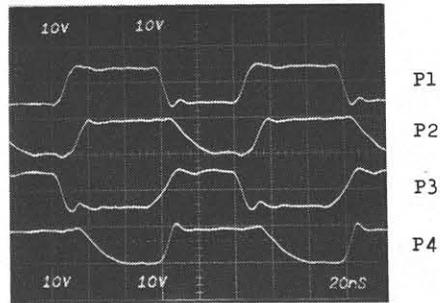


Fig.3(b) Clock Pulses of External Circuits

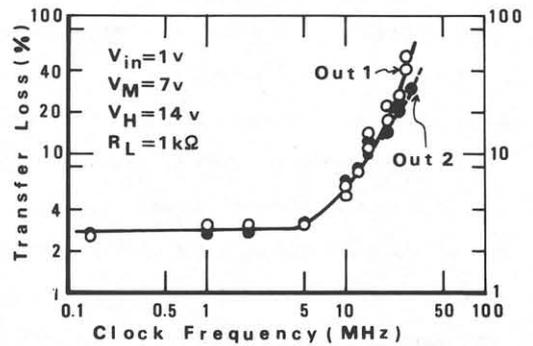


Fig.5 Charge Transfer Characteristics

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