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CCD With Meander Channel

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A CCD with two straight gate electrodes over a meander channel is proposed. The proposed CCD is suitable for transversal filters and clock line addressable memories because (a) the signal can be picked up at any point along the channel by a simple electrode without a crossover, and (b) only two discrete electrodes have to be driven for each channel. The bus lines which complicate the electrode pattern are absent.

The device structure is shown schematically in Fig.1. The channel is defined by interdigited channel stops. The gate electrode, 1 and 2, are parallel to each other, closely spaced and laid over an oxide layer covering the channel. The CCD cells are staggered along the device. Every other cell is under electrode 1 and the remainder under electrode 2. Each cell is devided into two parts. The oxide layer over the second part is made thinner than the first part to form a potential well in each cell. When the potential of electrode 1 is lowered, a charge in a cell under electrode 1 is transfered to the next cell under electrode 2. In the cell, the charge moves from the first to the second part and settles in the potential well. When the electrode potential is reversed, the charge is transfered to the third cell under

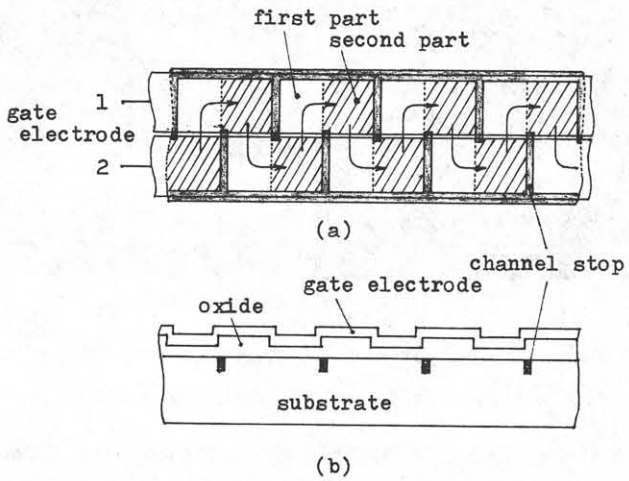


Fig.1 The basic structure of meander channel CCD. (a) a plan view. (b) a sectional plan view along the device.

electrode 1. Thus, when clock pulses are applied, the charge moves down the channel swaying between two electrodes as shown by arrows in Fig.1.

Several types of gate have been applied to this meander channel CCD of 32 bits. A photograph of one type of the shift registers is shown in Fig.2. The gate electrodes are made of stripes of poly silicon and aluminum and overlapped to each other for decreasing the instability associated with the gaps. The cell size is 60 x 30 μm^2.

The device was successfully operated in a both one- and two-phase mode and showed transfer efficiencies above 99.9% and 99.97% at 500 KHz, respectively. Fig.3 is an oscillograph showing the actual operation in each phase mode.

The device could be fabricated with a higher yield than that of conventional CCDs.

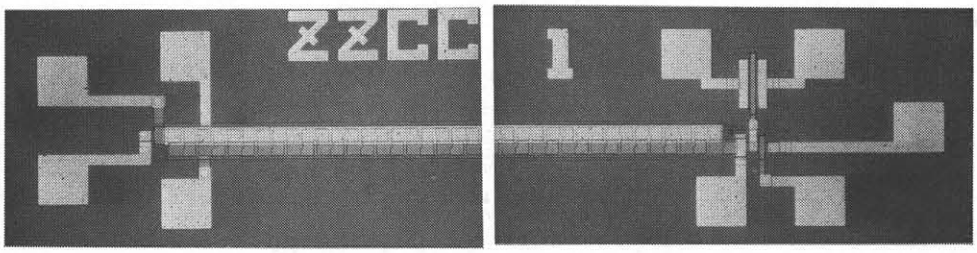
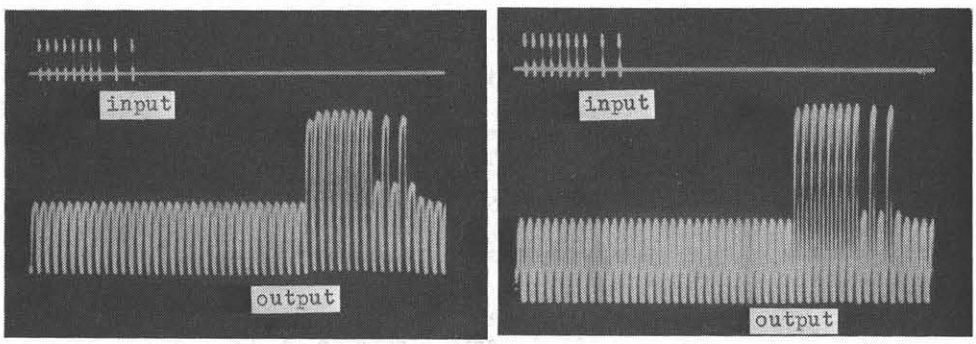


Fig.2 Photographs of the two ends of a fabricated CCD chip.



(a) (b)

Fig.3 Input and output signals from the CCD during operations in (a) one phase mode and (b) two phase mode, respectively.

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