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A-5-4 A NEW MULTIPHASE ELECTRODE-PER-BIT STRUCTURE FOR CCD MEMORY

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A new high density electrode-per-bit (E/B) structure known as multiphase serial parallel serial (MSPS), and its successful demonstration with a 4096-bit serial decoded CCD memory have been reported in our recent paper.(1) The substantial improvements are described with improved design and use of n-channel technology. The MSPS array is a combination of the E/B multiphase storage principle with the SPS structure which possibly achieves the highest storage density without requiring complicated external timing. In contrast with the normal 2-phase serial register in case of the standard MSPS array, an interlaced structure has been used to improve in density even more.

Fig. 1 shows the details of a 256-bit interlaced MSPS storage array along with its timing diagram. Clock levels shown are corresponding to surface potentials regardless to either p-channel or n-channel. The square symbol denotes a single charge storage site, which is a combination of a barrier electrode with a charge storage region, and a gating site S is a charge transfer region. Timing is indicated one pulse prior to the serial to parallel transfer of the next 4-bit data (N), where another 4-bit data (N) are loaded already. The input serial register is filled twice to fill the first parallel line, but stops on an alternate phase for each time. The propagation of control blanks (E) in position B8 during next 15 multiphase pulses, shift down all the data in parallel section one position, while the data (S) are unscrumbled by the final parallel line A4 and recirculate successively from the output register to the input register through the sense amp. and charge injector.

Fig. 2 shows an output data pattern at 1.0 MHz detected in analog, corresponding to a checkerboard inputs transferred through a 256-bit interlaced MSPS array. The chip was impremented in p-channel conductively connected CCD (C4D). The C4D structure offers the advantage of utilizing standard p-channel Si-gate technology, but mainly caused by channel modulation effect, the transfer efficiency is limited and also needs more area for conductive region.

To improve the problems above, an n-channel 2-level poly-Si gates CCD with ion implanted barrier to form the directional charge storage well (Fig. 3) has been studied and used in an experimental interlaced MSPS devices (Fig. 4). The typical charge transfer characteristics are compared in Fig. 5 for the same storage area of 90 μ^2. With proper fat "0" level ($\sim$15%), n-channel device can be

operated about 4 times faster, or alternatively at least 4 times larger array can be designed for the same clock frequency. The area per bit in the parallel section including the isolation is 224 μ^2 for this n-channel device while that of p-channel C4D is 374 μ^2, thus results in about 40% area reduction.

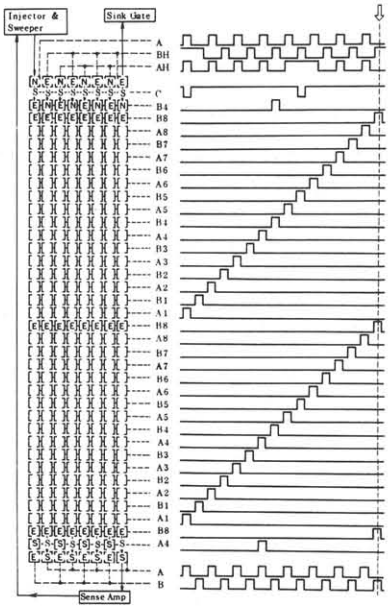

Fig. 1. Interlaced MSPS array and timing diagram.

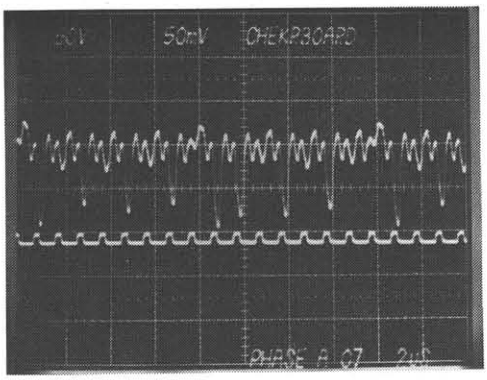

Fig. 2. Propagation of data pattern through a 256-bit interlaced MSPS array.

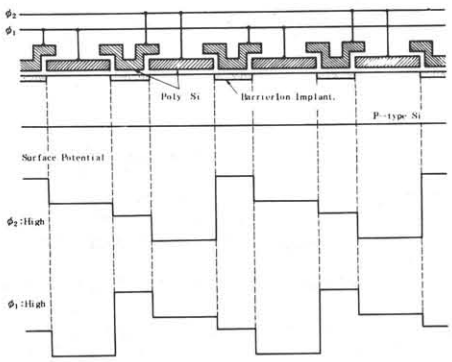

Fig. 3. N-channel 2 level poly-Si gates CCD structure with ion implanted barrier.

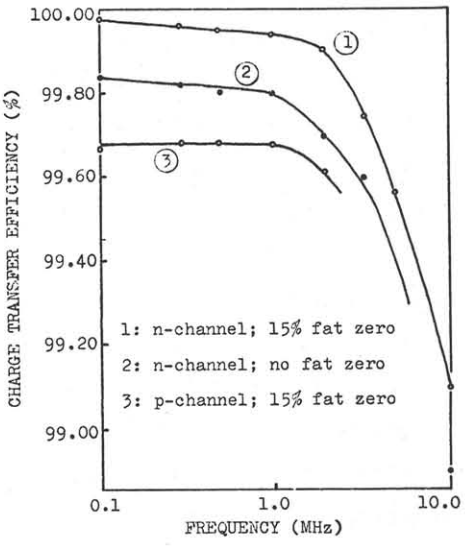

Fig. 5. Charge transfer characteristics of n-channel CCD and p-channel C4D.

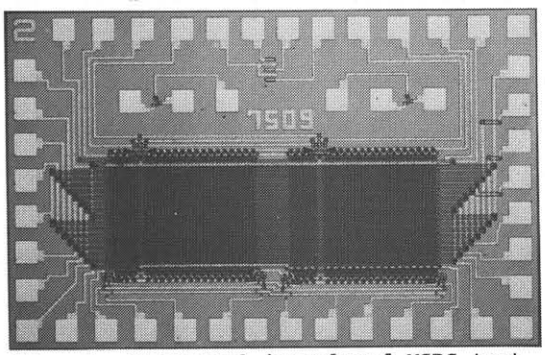

Fig. 4. N-channel interlaced MSPS test device 256-bit and 1024 bit arrays.

(1) W.E. Tchon, B.R. Elmer, A. J. Denboer, S. Negishi, K. Hirabayashi, I. Nojima and S. Kohyama: IEEE Trans. Electron Devices, Vol. ED-23, pp.93-101, 1976.