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A New Weighting Method for CCD Analog Sampled Filter*

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One of the most valuable application of the charge coupled devices (CCD,s) is the sampled data filtering of the analog signal. The advantage of using the CCD in such a filtering is that a very compact "semiconductor filter on-a-chip" can be produced, which has a probability to coexist with a large scale integrated circuit (LSI) of the signal processing systems.

It is the aim of this paper to propose a new weighting method for the analog sampled filter using CCD. A suitable block diagram to realize this CCD filter is illustrated in Fig. 1. The analog shift registers (A) are composed of buried channel CCD, which has a structure of poly-Si and Al overlapping gates. The operation mode of the CCD shift registers is four phase double clocking mode. The weighting blocks (B) are constracted of the respective input diodes and the double input gates. The weighted signals in these blocks (B) are transfered into the respective following shift registers arranged parallel to hold a distinct time interval among the respective weighted signals. These independently weighted and shifted signals are summed at the block (C). The weighting of the opposite sign is realized adapting the phase inverter of the analog signal (D). Thus the block diagram shown in Fig. 1 realizes the following non-recursive transversal filtering,

$$F(w) = \sum_{n=-N}^{n=+N} a_n . \exp(-j.n.w.T_c)$$

where, w is the frequency of input signal, $T_c=1/f_c$ is the sampling rate, f_c is clock frequency applied to the shift registers, a_n are weighting coefficients, and N corresponds to the order of this filtering.

The unique points of this constraction method shown in Fig. 1 are that the function of the weighting and sampling of the input analog signal can be formed simultaneously at the input area of the CCD shift register, therfore this method dose not need any improvement of the special technique to detect the weighted signals except the technique developed in an ordinary CCD shift register, comparing with the previously proposed methods which are application of the tap-weighting on one line CCD.

The weighting coefficients a_n of the blocks (B), that determines an arbitary response of the filter using CCD, have been calculated by the procedures used for the determination of the weighting coefficients in the case of the non-recursive digital filtering.

Fig. 2 shows the realized frequency response for the case of the low-pass filter. The cut-off frequency is designed one fourth of the sampling frequency f_c which corresponds to the clock frequency. As the number of the weighting coefficient is fifteen, the degree of this non-recursive filter is seventh order. The frequency f_c can be chosen up to 10 MHz. It is confirmed that this realized response of the low-pass filter has exhibited a reasonable agreement with the theoretically simulated response.

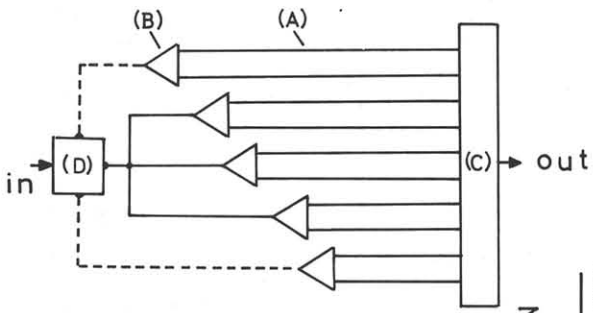

Fig. 1

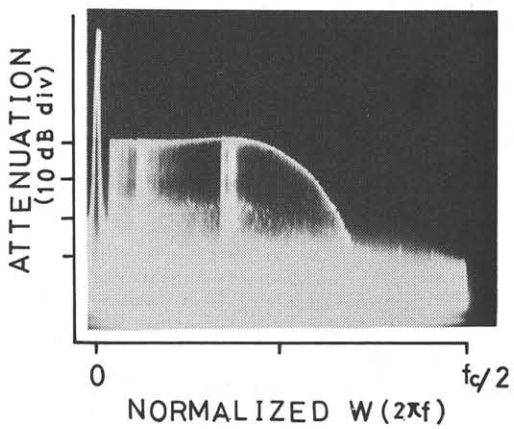

Fig. 2