

A-5-7

An Input-Weighted CCD Transversal Filter

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The potential of CCD transversal filters in signal-processing applications has widely discussed in the literature. A basic organization of the transversal filter is illustrated in Fig. 1. For constructing such a transversal filter using CCDs, the tapped delay line or the split electrode technique has been used.

CCDs have a summing function in addition to an analog time delay. Using the function, it is possible to organize a new type transversal filter as illustrated in Fig. 2. In this filter, the input signal is multiplied beforehand by weighting coefficient. Such an input-weighted transversal filter need not alter the basic CCD structure, only adding the weighting circuit. Therefore, it is advantageous that the device structure is very simple and there is no necessity for an external summing circuit. A further advantage is that the excellent frequency characteristics is expected since the device has no taps using floating diffusion or floating gate technique.

A 64-stage experimental device of that filter which is electrically reprogrammable was built and evaluated. A construction of the device is illustrated in Fig. 3 and a photomicrograph of the device is illustrated in Fig. 4. In the

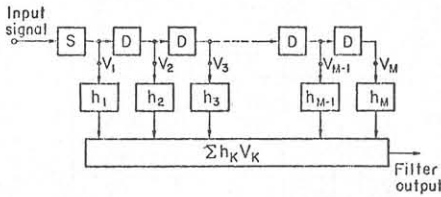


Fig. 1 Basic transversal filter

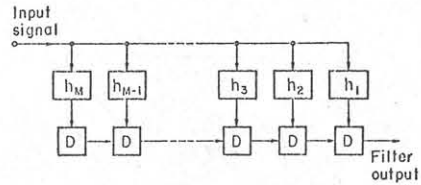


Fig. 2 Input-Weighted transversal filter

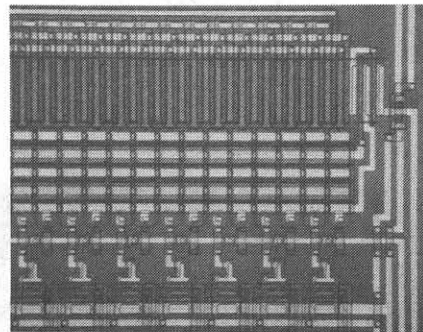
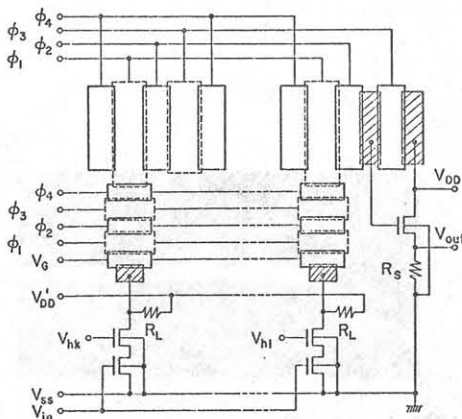


Fig. 4 Photomicrograph

Fig. 3 Device construction

device, dual gate FETs are used for the input-weighting and 4-phase surface n-channel CCD is used for the time delay and summing, which are monolithically integrated on a 3.6 x 2.2 mm chip. The device was fabricated using a self aligned, two-layer polysilicon, standard CCD process except ion-implantation technique for making load resistors of the FETs.

In Fig. 3, the branched input signal is applied to one gate of each dual gate FET and, to another gate, the weighting voltage V_{hk} corresponding to the weighting coefficient h_k is applied. The signal current which is controlled by V_{hk} flows through the load resistor and consequently the weighted signal occurs at both ends of the resistor. The weighting characteristics of that dual gate FET is illustrated in Fig. 5 in which DC offset voltage of the input signal (V_{inDC}) is used as a parameter.

The weighted signal is applied to the CCD source and sampled by 1-bit CCD. The sampled signal is introduced in the CCD delay stage and summed there to the signal transferred from the before delay stage. By this procedure at each delay stage, the filter output is finally obtained at the floating diffusion pre-amplifier.

Figure 6 illustrates a frequency characteristics as a delay line for 2- and 50-stage input. From the characteristics, it is evident that the device is adaptable for the video-signal processing. Figure 7 illustrates an impulse response and a spectral response for the transversal filter with Gaussian weight. By selection of the weights, other various kinds of filter can be obtained.

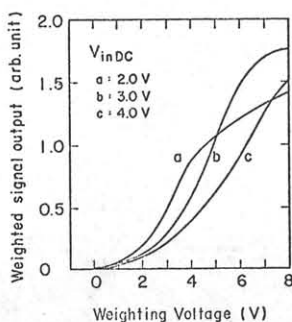


Fig. 5 Weighting characteristics

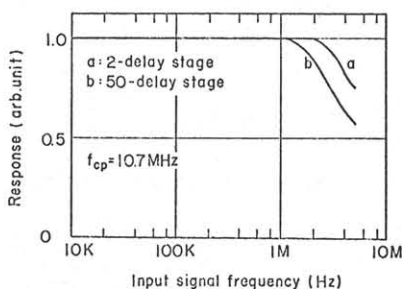
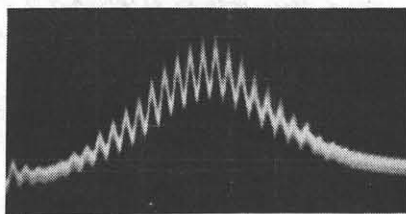
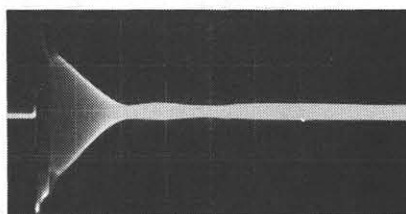


Fig. 6 Frequency characteristics



(a) Impulse response



(b) Spectral response

Fig. 7 Gaussian weighting filter