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Improvement of Planar GaAs Devices by Controlling the Properties of the Epilayer and the Epilayer - Substrate Interface.

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Planar Schottky-gate GUNN devices fabricated from GaAs-layers prepared in the conventional LPE way (i.e. growth from a supersaturated Ga-melt) on Cr-doped GaAs-substrates show an anomalous decrease of the prethreshold and the valley current during the transition from pulse to dc bias. In many cases the dc current saturates before reaching the threshold voltage. In extreme cases no high field domains can be triggered as shown in fig.1a. These effects can be explained by assuming

- 1) that electrons are trapped in the substrate near the interface, generating a depletion region in the n-layer
- 2) a conductive layer in the substrate near the interface, which enhances the thickness of the depletion region.

Since it was supposed, that the long heat-treatment of the semiinsulating substrates prior to the epitaxial growth causes these effects, more investigations of the LPE process were necessary.

A long heat-treatment of the melt is necessary to obtain high-purity layers and to prevent morphological defects like holes (30 - 40/um  $\phi$ ) in the epitaxial layers. In conventional LPE processes the substrate and the melt are at the same temperature.

Therefore intensive investigations using the SEM, microprobe, AUGER-spectroscopie, HALL-, breakdown voltage-, capacitance-voltage-, thermally stimulated capacitance measurements were made on heat-treated Cr-doped GaAs-samples. After a 2 hours heat-treatment of the substrate in purified hydrogen at 700°C the sample surface had converted to n-type with  $9<1 \,\Omega\,\text{cm}$ ,  $/u_{\rm H} = 2500 \,\text{cm}^2/\text{Vs}$ , n =  $5.10^{16} \,\text{cm}^{-3}$ , N<sub>T</sub> =  $2.10^{16} \,\text{cm}^{-3}$  and several trap energy levels.

Among several possibilities for an improvement of the LPE process, a melt-back of the disturbed substrate surface in an unsaturated Ga-melt prior to the growth was used. For this purpose a new rotatable graphit slider boat was constructed (fig.2). Morphological defects are almost completely removed and the transition of the conductivity from the epilayer to the substrate is nearly ideal (fig.3).

GUNN devices made from such layers hardly show any difference between pulse and dc operation (fig.1b).





Current-voltage characteristics of a planar GUNN device under pulse and dc bias

a) fabricated on a wafer grown by a conventional LPE process



fig.2 Rotatable graphit slider boat for 3 melts. Substrate dimensions 30 mm x 15 mm.



fig.3

Electron concentration as a function of depth from the sample surface.