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A Half-micron Gate GaAs FET Fabricated by Chemical Dry Etching

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The GaAs Schottky barrier gate FET has occupied the premier position of microwave transistors, especially in the higher GHz range. Intense demand for the improvement of the performance as well as use at higher frequencies has forced the technological requirement beyond the limit of conventional technolo -gy. Microfabrication of the Schottky gate is of primary importance and a half-micron gate is destined to be a vital topic in this field. In order to get better gigh-frequincy performance, microfabrication technique should be compatible with the following requirements; (1) reproducibility (2) accurate duplication (3) easiest lithographic technique (4) minimal introduction of capacitive and resistive parasitecs. There have been several attempts to make a submicron gate structure. Electron-beam exposure or electron-beam mask-making was one of the solutions. However, the direct exposure method does not satisfy requirement (3) and both, if combined with the lifting process, fail with respect to requirement (4). On the other hands, wet chemical etching was not compatible with requirements (1) and (2).

Consequently, we have attempted to use chemical dry etching to meet the above four requirements. The minimum geometric length of the photomask need only be one micron. In addition, ordinary photolithographic techniques can be applied to duplicate the one-micron pattern on the photoresist film deposited on the thick metal layer. Undercutting the metal produces submicron contact with the semiconductor, leaving a wider top surface of the metal.

Half-micron gate GaAs FET's were fabricated by the above idea. High gain and low noise requirements have demanded additional new technologies. Good epitaxial crystal and low resistance ohmic contacts are realized by growing a triple layer (n^+ - n - buffer) on a semi-insulating GaAs substrate. Reduction of the parasitic capacitance by appropriate electrode geometry design was also important.

The n-type epitaxial layer was grown by the vapor reaction of $Ga/AsCl_3/H_2$ with a carrier concentration of $8\text{-}10 \times 10^{16}$ cm^{-3} and a thickness of 0.2-0.25 μm. The buffer layer was p-type with the carrier concentration around 5×10^{13} cm^{-3} and the top n^+ layer had a carrier concentration above 10^{18} cm^{-3}. The planar geometry of the electrode is shown in Fig 1. Ohmic contacts of source and drain were evaporated and alloyed Au-Ge, with Au on top and Ni in between.

A $NH_4OH-H_2O_2-H_2O$ mixture was used to etch the GaAs layer precisely, because it has a low etching rate of around 0.1 µm/min. The Schottky barrier gate was evaporated Mo with Au on top. The top metal was first delineated by ion milling with the 1 µm photoresist mask. The Mo layer was chmically etched in CF_4 gas plasma. Controlled side etching of Mo yielded the submicron gate with no shrinking of the Au layer. The SEM observation of the detailed gate structure is shown in Fig 2.

The submicron gate GaAs FET was mounted in a ceramic disk package. The gain and noise figure are plotted in Fig 3 against the frequency. The maximum frequency of oscillation as high as 80 GHz was observed. The noise figure was only 2.3 dB at 7.4 GHz and 3.3 dB at 12 GHz. Maximum available gain was 17 dB at 8 GHz and 13 dB at 12 GHz. Electrical measurement and visual inspection confirmed a gate length of 0.5 µm. Resistance of the gate metal was smaller than the 1 µm gate GaAs FET fabricated by the lifting process. Some adverse effects were thought to exist because of the presence of high energy ions. However, the high frequency performance was improved in accordance with the gate length and no definite disadvantage could be found in the process, even in other respects.

It could be concluded that the chemical dry etching is a plausible method for submicron pattern microfabrication. A half-micron gate GaAs FET with superior performance was fabricated by combining this technology with a novel crystal structure and new geometrical design.

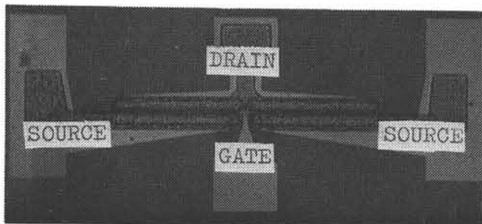

Fig 1. Top view of a submicron gate GaAs FET

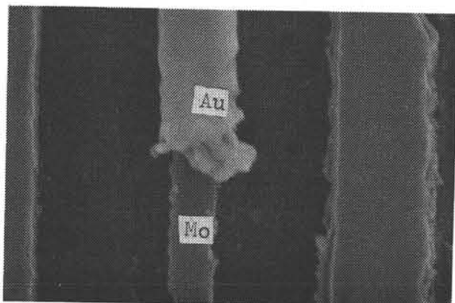

Fig 2. The SEM photograph of the gate structure (Top metal Au is partly stripped off)

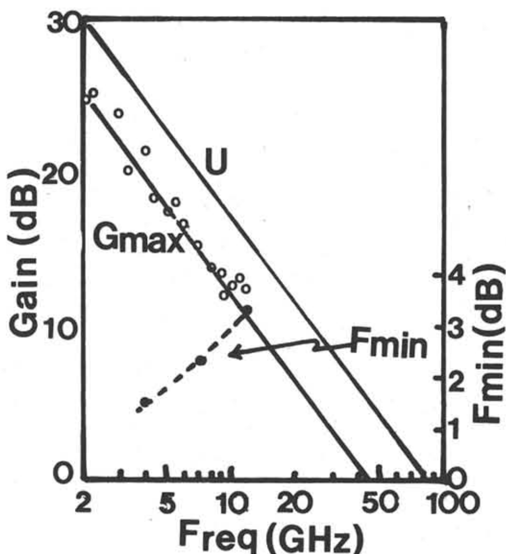

Fig 3. High frequency performance of a 0.5 µm gate GaAs FET