C-3-2

A New Isolation Technique for SOS/LSIs

— Local Buried Oxide Isolation of SOS (LOBOS) —

Yoshio Sakai, Ryoichi Hori, Kikuo Dota and Masaharu Kubo

Central Research Laboratory, Hitachi Ltd.

Kokubunji, Tokyo, Japan

SOS(Silicon on Sapphire) technology has a number of advantages in achieving high performance MOSLSIs. However, it suffers from poor controllability of the threshold voltage caused by outdiffusion of Al, and low yield due to interconnection defects caused by the steps. The LOCOS(Local Oxidation of Silicon) technique could avoid some of the drawbacks of the conventional SOS processes. However, the long oxidation step at high temperatures(>1000°C) needed in the LOCOS process results in undesirable impurities and stress in the silicon film, which makes SOS devices more leaky. Consequently, a low temperature processing technique for SOS/LSIs needs to be developed.

In this paper we describe a new self-aligned oxide isolation technique which gives high yield SOS/LSIs. The new technique utilizes thick SiO_2 film grown by chemical vapor deposition at low temperature(<500°C) as field oxides which are buried between the silicon islands, and is called Local Buried Oxide Isolation of SOS(LOBOS). The key processing steps are shown in Fig.1. The photoetching process utilizes the fact that for ultraviolet light($3500\text{Å}<\lambda<4300\text{Å}$) both the sapphire and the SiO_2 film are transparent, but the silicon film(~1μm) is opaque. Therefore, the negative photoresist on the SiO_2 film deposited on the sapphire substrate is exposed to the ultraviolet light projected from the back surface of the sapphire substrate, but the photoresist on the silicon film is not. After dissolving the unexposed photoresist on the silicon film, the thick SiO_2 film on silicon islands is removed by chemical etching. Through these simple photoetching steps, the LOBOS structure is realized.

Fig.2 shows the step height of LOBOS and the conventional structure measured by "Taly step". It is seen that the step height is reduced to less than 1000 Å with the LOBOS technique. Fig.3 shows scanning electron micrographs of the fabricated silicon-gate SOS/MOSFET. In the LOBOS structure, polycrystalline silicon wirings encounter much smaller difference in height at the edge of the silicon islands than in the conventional case, which makes it possible to form finer patterns. A shallow groove is observed at the oxide-silicon transition in LOBOS I. This groove can easily be removed by proper annealing and the surface is completely planed in LOBOS II.

Typical device characteristics of n-channel SOS/MOSFETs with LOBOS structures(LOBOS/NSOS) are summerized in Table I together with those of conventional structures(Conv./NSOS). The threshold voltage V_{th} is lower and the channel conductance(or mobility) is about 5 % larger in LOBOS/NSOS than that in Conv./NSOS. These are considered to be due to the negligibly reduced outdiffusion of Al during the device processing of LOBOS/NSOS.

The leakage current in LOBOS/NSOS is the same as in Conv./NSOS. This indicates no increase in contamination or stress in LOBOS/NSOS.

The following features are the advantages of the developed LOBOS technique:

(1) Reduction of the step height, which gives good interconnections and allows fine patterning.

(2) Prevention of diffusion of impurities from sapphire into the silicon film, which results in the small leakage current and improved threshold voltage controllability.

(3) Elimination of parasitic MOS transistors at side walls of the silicon islands.

(4) Prevention of dopants from diffusing to the side walls of the silicon islands, which makes it easier to realize short channel devices with high punchthrough breakdown voltage.

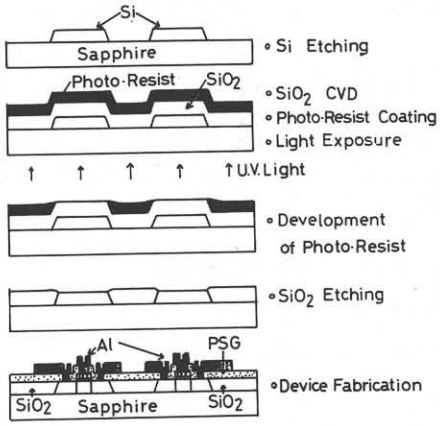
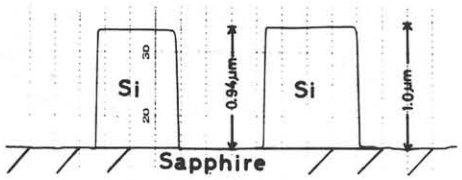


Fig.1 Processing steps of silicon-gate SOS/MOSFET with the LOBOS structure.

The authors wish to thank Mr.N.Hashimoto, Mr.T.Masuhara and Mr.N.Hasegawa for their helpful discussions.



(A)Conventional Structure

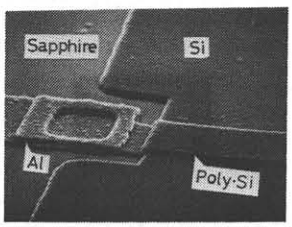
(B) LOBOS Structure

Fig.2 Step height of Conventional and LOBOS structure measured by "Taly step".

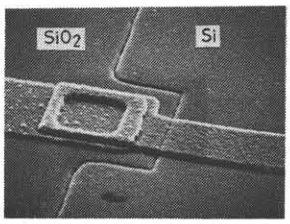
Table I Device characteristics of LOBOS/NSOS and Conv./NSOS.

	V_{th} (V)	β_o ($\mu\Omega$/V)	I_{leak} (pA/μm)
LOBOS/NSOS	2.5~2.65	5.7~6.7	0.95~2.0
Conv./NSOS	2.7~2.8	5.3~6.4	0.53~2.3

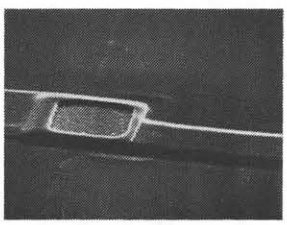
V_{th}:Threshold Voltage
β_o :Unit Channel Conductance
I_{leak}:Leakage Current per unit channel width



(A) Conventional Structure



(B) LOBOS I



(C) LOBOS II

Fig.3 Scanning electron micrographs of Conventional and LOBOS structures.