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# A 2400-gate RALU on SOS

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This paper describes high speed 2400-gate random logic LSI on SOS chip. The LSI consists of 16-bit Register and Arithmetic Logical Unit named RALU, which is fabricated by means of n-channel Si gate E/D technology.

For a random logic, n-channel E/D gate is more superior to CMOS gate from a view point of design simplicity and packing density.

The epitaxial Si films grown on sapphire substrate are P type, highly resistive, (100) oriented and 1 $\mu$ m thick. Gate oxide thickness is 1000 $\text{\AA}$ . Ion implantation technique is applied to accurately control the threshold voltage of E-mode Tr. and D-mode Tr.<sup>1)</sup> The photolithographic channel length is 6 $\mu$ m.

Figure 1 shows the block diagram of RALU, which consists of Local Storage (LS) and ALU. This device is operated with a single +5V power supply ( $V_{DD}$ ) and a single clock. LS consists of sixteen 16-bit registers, two 4-bit address stack pointers and increment/decrement circuit of addresses. The repertoire of ALU are LOAD, STORE, ADD, SUB, REV.SUB, AND, OR, XOR, SHIFT L or R, BRANCH and HALT. Since LS block and ALU block are combined to common bus lines, RALU exchanges data internally. Therefore, only adding external controls does make RALU a micro-processor. A photomicrograph of the chip is shown in Fig. 2. Chip size is 5.00mm x 4.72mm.

Figure 3 shows access time of LS vs.  $I_{DO}$ .  $I_{DO}$  is the current of a load transistor ( $W/L = 6\mu\text{m}/6\mu\text{m}$ ) at  $V_{OUT} = 0\text{V}$  (defined in Fig. 3). Therefore,  $I_{DO}$  is a parameter of the device power dissipation. Access time is measured from the leading edge of the clock input (which initiates the word line selection) to the data output value at 2.4V. The shortest access time is 74 nsec. in the  $I_{DO} = 108\mu\text{A}$  to 118 $\mu\text{A}$  range. Figure 4 is an oscillograph of the access time.

Figure 5 shows the propagation delay time in the carry circuit through 11 gates, from bit 0 to bit 15, as a function of  $I_{DO}$ . The filled circles show SOS and open circles show bulk silicon with the same dimension. As the propagation delay is a suitable criterion of that of ALU operation, the delay on SOS is compared with that on bulk silicon at the same power dissipation. The SOS delay is 50 nsec. and that of bulk silicon is 90 n sec. at  $I_{DO} = 125\mu\text{A}$ . The difference in the two delays should be due to a lack of parasitic capacitances and substrate bias effect, the latter effect is estimated to be  $\sim 40\%$  of the difference in the delays.

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# Reference

- 1) H. Tango, J. Iwamura, K. Maeguchi, M. Isobe: Proc. 6th Conf. Solid-State Devices (1974) Tokyo, Japan p.225

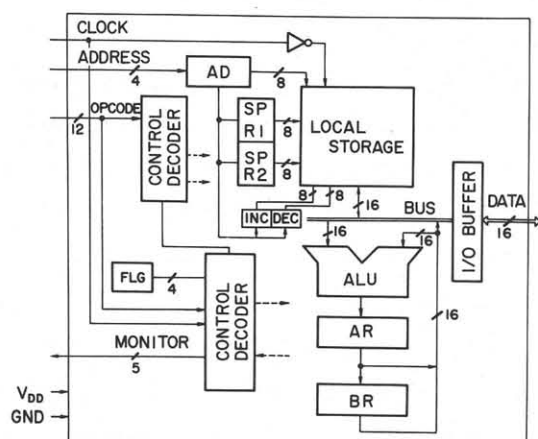


Fig.1 Blockdiagram of R-ALU

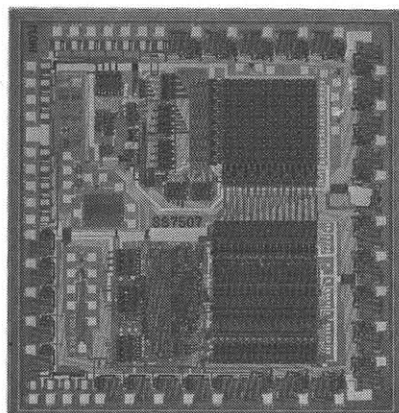


Fig.2 Photomicrograph of RALU

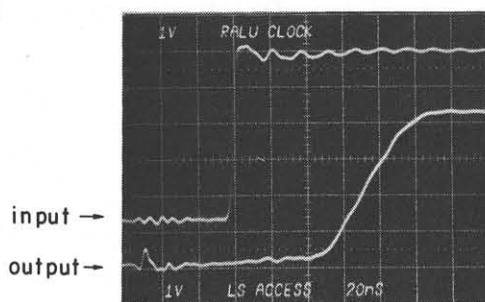


Fig.4 Oscillograph of Access time  
VERT : 1V/div.  
HORZ : 20nsec./div.

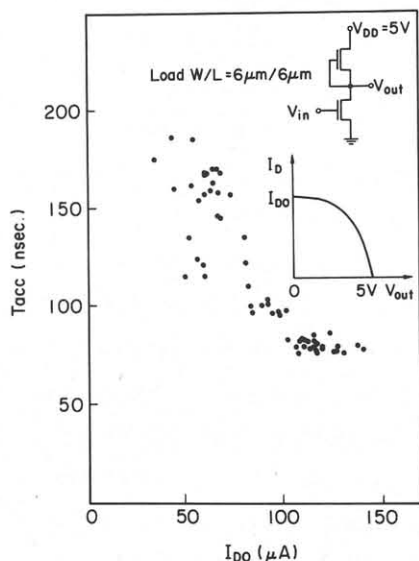


Fig.3 Access time of Local Storage vs. I<sub>D0</sub>

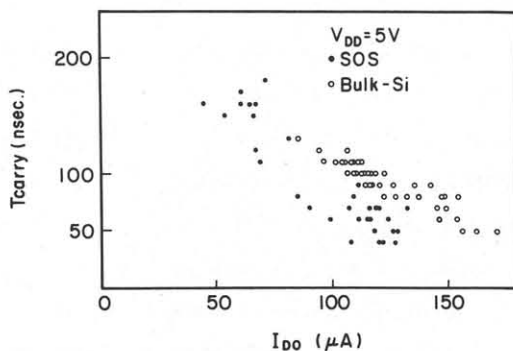


Fig.5 Propagation delay of carry from bit 0 to bit 15