A—2—1 (INVITED) Physics and Device Technology of Silicon on Sapphire†

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Because of a number of heavy limitations concerned with physical, technological and economical aspects, silicon on sapphire technology, SOS, had required quite a long runway to take off. However, recent rapid progress in device technology has powerfully promoted practical realization of SOS integrated circuits as (1) CMOS/SOS, (2) n-MOS/SOS and (3) other novel devices, as well as physical understanding and further improvements in materials and processings. The first category involves a microcomputer, a 1024 bit static memory, a logic with a small number of gates, a watch circuit etc. The second one is mostly for a microcomputer and several functional blocks. The third one involves a nonvolatile memory and several display devices combined with, for instance, a liquid crystal display. The primary difficulties of the SOS structure, such as obtaining the epitaxial film with acceptable electrical properties, and with reasonably good crystal perfection, seem to be solved from the practical point of view for fabrication of MOS integrated circuits on SOS substrate. Thus, SOS is now coming into the arsenal of silicon integrated circuits technology. In other words, SOS has grown up to be an object which has to be compared with the other well-established silicon technologies for the cost performance.

Basic superiority of the SOS structure to the bulk silicon structure should be in a lack of parasitic capacitances of both diffused layers and aluminum and/or polycrystal silicon layers with respect to the substrate. This is, indeed, confirmed through n-channel MOS LSI on SOS substrate, and CMOS LSI on SOS substrate, both of which have given rise to better performance and higher packing density compared with those on bulk silicon substrate. However, there still remain a number of phenomena which should be revealed prior to further development of SOS technology.

This paper reviews the present status of SOS, and discuss future possibility of SOS LSIs with emphasis on the following subjects.

(a) SOS wafer, the present and future trends in material and processing cost.
(b) Physical limitation to the carrier mobility in epitaxial silicon layer.
(c) Characterization of SOS wafer, role of crystal defects in silicon and on sapphire substrate on the physical and electrical properties of silicon layer.
(d) Device characteristics of MOS FET on SOS wafer, reduction in junction

capacitance, lack in the substrate bias effect etc.

(e) Comparison of SOS LSI with the other bulk LSIs for several basic circuit configurations.

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