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A 64K MOS RAM Design

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A 64-kbit dynamic MOS RAM, capable of 200 ns access time and 150 mW power dissipation, has been developed using a single transistor cell and a single-level N-channel polysilicon gate process.

The 64K is organized as a 16 kw x 4 bit RAM. A block diagram of the 16K is shown in Fig. 1. Figure 2 shows a photograph of the whole chip. A sense circuit array is located in the center of each 16K block. 64 memory cells are connected to each of two nodes in a sense circuit symmetrically. All signals and clocks are TTL compatible. The refresh cycles are 128. Dimensions of the single-poly cell and whole chip are 14 μm x 15 μm and 6.1 mm x 5.8 mm, respectively.

The small memory cell and the extremely low power dissipation are mainly attributed to a novel sense circuit. The proposed sense circuit, memory cells and dummy cells are shown in Fig. 3(a). Figure 3(b) shows the simulated waveforms of internal clocks and those at several nodes in the sense circuit. The sense circuit operates as follows: All bit lines are precharged to the reference level ($\fallingdotseq$ 2 V). The memory cell signal is transmitted to a flip-flop circuit through a switching transistor, inserted between bit line and flip-flop circuit, by selecting a word line. As the switching transistor operates in the triode region, the signal is transmitted rapidly. After the switching transistors turn off, the transmitted signal is amplified in the sense circuit, while all bit lines are independently charged up to a high level. Then, the switching transistors turn on again and either node capacitor on the bit line is discharged, according to the latched signal in the sense circuit.

This sense circuit is very sensitive, because the switching transistors can disconnect the bit line capacitor from the flip-flop circuit at detecting time and eliminate the effect owing to the bit line capacitor dispersion. It has been verified that this sense circuit can detect a signal smaller than $\pm$30 mV. The signal transmitted from the cell to the bit line is designed to be $\pm$100 mV for the 64K in the worst case. As the static current does not flow in this sense circuit, low power dissipation, 80 μW/sense circuit, is realized. DC supply voltages are 7 V and -2 V. The proposed sense circuit, low power peripheral circuits and low DC supply voltages make possible developing extremely low power 64K device, 150 mW at 500 ns cycle time.

Features of a MOS transistor are 2 μm effective channel length, 500 Å gate oxide thickness, 0.25 μm junction depth and 0.8 V threshold voltage at 1 V drain voltage.

Figure 4 shows 64K waveforms. Key device characteristics are summarized in Table 1.

The technologies employed in the 64K fabrication are as follows: As-doped polysilicon gate, selective oxidation, Mo metallization, all ion implantation, flowed phospho-silicate glass and fine pattern technology using photolithography (2 μm minimum pattern width).

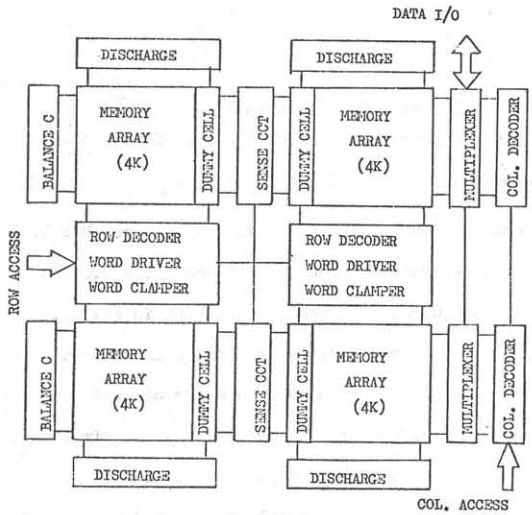


Fig.1 16K Block Diagram in 64K

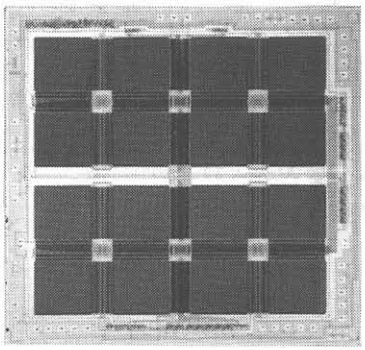
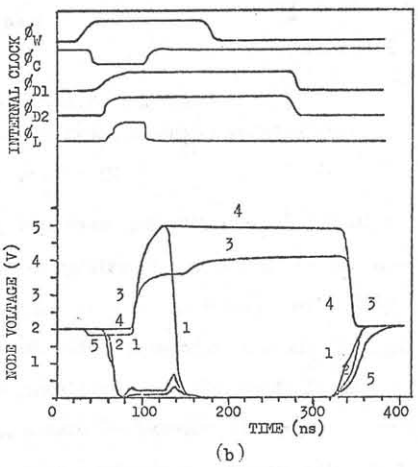
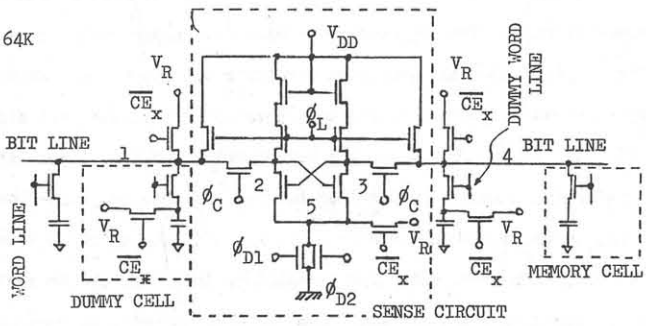


Fig.2 64K Chip Photograph



(b)



(a)

Fig.3 Sense Line Circuit and Simulated Waveforms of Clocks and Sense Circuit Nodes (1~5)
(a) Sense Line Circuit (b) Simulated Waveforms

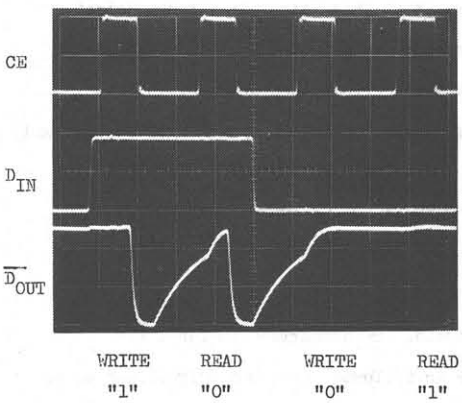


Fig.4 64K RAM Timing and Waveforms
Vertical Scale - 2V/div.
Horizontal Scale - 200ns/div.

TECHNOLOGY	SINGLE-POLY CELL, N-CHANNEL Si-GATE
ORGANIZATION	16 kword x 4 bit
CELL SIZE	14 μm x 15 μm
CHIP SIZE	6.1 mm x 5.8 mm
ACCESS TIME	200 ns
CYCLE TIME	500 ns
SUPPLY VOLTAGE	+7 V, -2 V
OPERATING POWER	150 mW
STANDBY POWER	10 mW
REFRESH	128 CYCLES/2 ms
I/O INTERFACE	TTL (INCLUDING ALL CLOCKS)

Table 1 Typical 64K Characteristics