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High Performance 4k Dynamic RAM Fabricated with Short Channel MOS Technology

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A 4k dynamic RAM has been designed utilizing a newly developed short channel MOS technology. The MOS RAM features a typical access of 90ns and a power dissipation of 40mW at a single 5-V supply.

The short channel MOS technology uses polysilicon gate lengths of less than 3μm and a gate oxide thickness 50nm. Shallow junctions of less than 0.5μm are obtained by using arsenic as the source-drain diffusant. This enables the use of a high resistivity substrate (≃10Ω·cm) that is effective in obtaining shorter access time.

Like its forerunners, this MOS RAM uses the basic one-transistor per cell[1] having an area of 16x24 μm^2 as shown in Figure 1. This is about 2/3 of the standard 5μm technology. The memory is organized as a 4096x1 bit RAM. The die size measures 8.4mm^2.

Reducing the physical dimensions of the MOS transistor decreased the source-drain breakdown voltage to 11V. Consequently, the MOS RAM can not be operated with a usual supply voltage; V_{DD}=12V±10% and V_{BB}=-5V±10%. For this reason, the RAM is designed so that it works with a single 5-V supply.

Access time and power dissipation of the MOS RAM are plotted as a function of the supply voltage V_{DD} in Figure 2. An access time of 90ns, power dissipation of 40mW, and access power product of 3.6nJ have been obtained at V_{DD}=5V. The access power product of 3.6nJ is about 1/6 to 1/8 lower than the same MOS RAM with a conventional 5μm channel devices (V_{DD}=12V, V_{BB}=-5V). Standby power dissipation was reduced to under 1mW.

Memory storage time T_{st} vs. substrate bias V_{BB} is shown in Figure 3. T_{st} corresponds to the worst bit in the array. In spite of the 60% reduction of the stored "1" voltage in the cell compared to the conventional RAM, memory storage time at V_{DD}=5V is almost the same as the conventional RAM operated at V_{DD}=12V. This is due to the low power dissipation of the RAM. The figure indicates the RAM can be used with a usual refresh interval spec that is 2ms at V_{DD}=5V.

The short channel MOS technology makes possible extremely low minimum operating supply voltage of 4V. As a result, the RAM can be operated with a 5-V single supply without substrate bias generator.

The design and processing technology in this report should provide a basis for future large capacity MOS RAM. Capacities of 65k bit or 128k bit per chip with short access time and much smaller power dissipation will be feasible.

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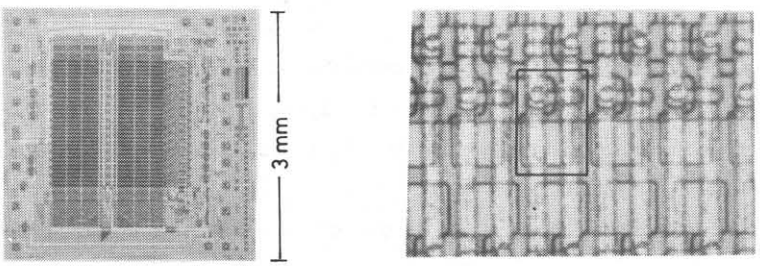
Reference

(1) K. Itoh et al. : IEEE J. Solid-State Circuits, vol.sc-11, no.5, pp 585-590, Oct. 1976



(a) (b)

Fig.1 Photomicrograph of a 4096 bit dynamic MOS RAM (a) and one-transistor per bit cell (b)

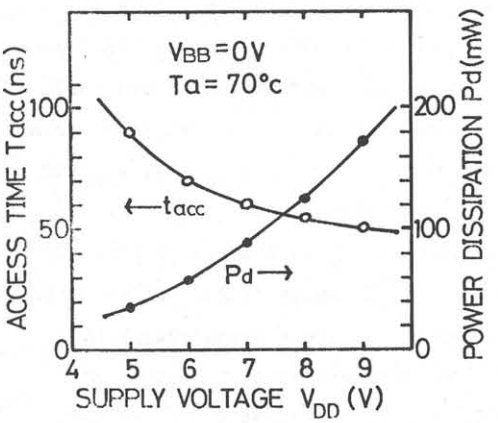


Fig.2 Access time and power dissipation of the RAM as a function of the supply voltage V_{DD}

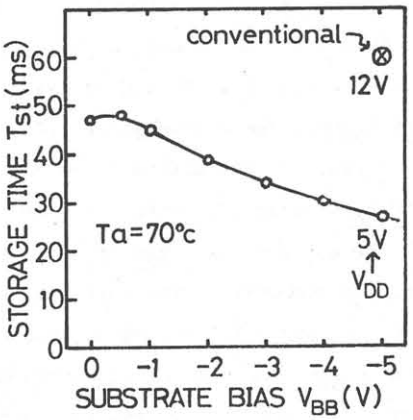


Fig.3 Memory storage time T_{st} vs. substrate bias V_{BB}