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High Speed 4K Static RAM using DSAMOST's

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A high speed, fully static, 1024 word by 4 bit Random Access Memory has been developed, using Diffusion Self-Aligned (DSA) MOS transistors[1] as active devices.

The present RAM operates on a single power supply of 5 (±1) volts without internal bias generator. Its typical performances are; access time 57nsec, cycle time 100nsec and operating power 520mW. The device was also confirmed to operate satisfactorily in the battery back up mode with 4.4mW (V_{DD}=1.1 V) power dissipation.

Figure I shows a cross section of the DSA ED MOS inverter integrated in the RAM.

Silicon gate device structure with reduced dimensions was combined with the advanced local oxidation technique to realize the high speed operation of the RAM.

In DSA devices with less than 2 μm source-drain separation, gate oxide of about 800 Å thickness and source and drain regions of about 1 μm depth were used without any problems of short channel effects. Measured gain constant β magnitude is about 90 μ℧/V, for 10 μm gate width. The DSA MOST threshold voltage was tightly controlled within 1.0±0.1 volt by use of the refined ion-implantation technique. The p-type diffused layer for the channel stopper was vertically separated from the source and drain n^+ regions, as is shown in Fig.1. Together with the high resistive (100Ωcm) substrate used, this devised isolation structure substantially reduced the junction capacitance leading to the high speed operation of the device.

In the load device, two types of load MOST's with different threshold voltage (V_{TL}) values, which were adjusted by ion-implantation technique, were used to meet the high speed and low power requirement; one with V_{TL}=−3volts for write driver and decoder, and the other with V_{TL}=0 volt for decoder buffer and cell load.

The 1024 word by 4 bit static memory circuit was designed as follows: (1) Chip Enable (CE) circuit is made up of multiple connected ED inverters. CE circuit generates internal clock pulses. (2) Address, chip select and data buffers are flipflop type latch circuits. They are clocked by CE signals. (3) X,Y decoders are conventional NOR gates. Decoder buffers are push-pull circuits. As the decoder buffer, a push-pull circuit with 0 volt gate threshold load MOST was used. (4) Memory cell is the conventional 6 Tr. Cell. The load current is limited to under 1 μA. (5) For sense amplifiers, balanced differential amplifiers were used. (6) Data-in buffers and write drivers were constructed using the ED inverters and push-pull circuits. Figure 2 shows CE input and read-out signal waveforms. Figure 3 shows read access time V_{DD} dependency, and Figure 5 shows a DSA 4K static RAM chip microphotograph. Typical characteristics of 4K RAM are summarized on Table 1.

In conclusion, a high speed static 4K RAM with reasonable operating margin has been developed using DSA MOST's. The process technologies used are not critical ones and applicable to its production.

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1) Y. Tarui etal., Proc. 1st Conf. Solid State Devices, Tokyo, 1969.

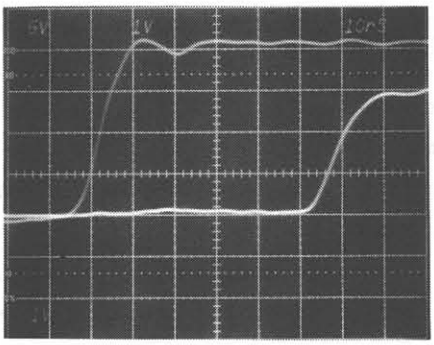

Fig.2 Chip enable signal(a) and read-out signal (b) waveforms (V_{DD}=5 V)

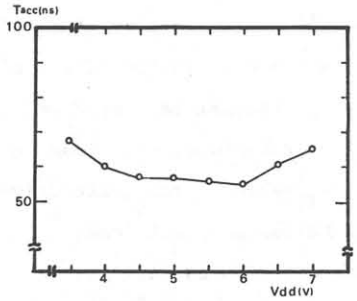

Fig.3 Read access time V_{DD}dependency

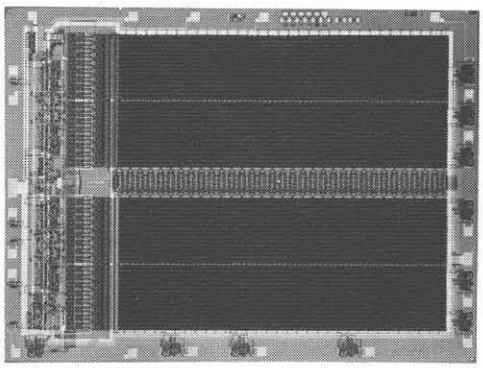

Fig.5 A DSA 4K static RAM chip microphotograph

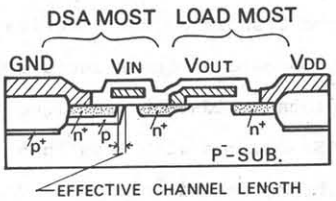

Fig.1 A DSA ED inverter cross section

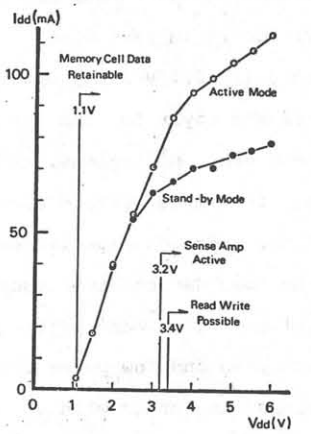

Fig.4 Total current (I_{DD}) V_{DD}dependency

Technology:	N-channel Si gate, π planar DSA ED MOS, vertical separation
I/O:	I/O common and Tri-state output
Pins:	22 pins
Chip size:	4.6 x 6.09 mm^2
Organization:	1024 word by 4 bit , fully static
Cell structure:	6 Tr. static cell
Power supply:	5 V single
Signal level:	TTL compatible
Read access time:	57 ns (25°C) 52 ns (0°C)
Cycle time:	100 ns
Power dissipation:	520 mW at active mode, 375 mW at stand-by mode

Table 1 4K RAM typical characteristics summary