Digest of Tech. Papers The 9th Conf. on Solid State Devices, Tokyo

A—6—1
(INVITED)

Static Induction Transistor Logic

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Introduction Static Induction Transistor (SIT) was invented in 1971[1], but idea of multichannel field control transistor, including forward gate bias, had been published in 1950[2] followed by Shockley in 1952 as analog transistor[3].

As a result of the reduction of the series channel resistance R_s of the field effect transistor (FET), the V-I character changes into the exponential from the saturating[4,5]. This also ascertained that the saturation character appeared based on the negative feedback action through R_s. Therefore, the FET is rather extrinsic transistor including excess feedback resistance connected in series with SIT, which is thought rather as intrinsic.

The main normal mode of SIT is in pinched-off condition, therefore the main mode of SIT starts from the cut-off in usual V-I character of the FET, which means $I_D \simeq 0$. And with the increase of the drain voltage, pinched-off barrier is lowered by the static induction from drain, increasing the flowing drain current.

If compared with bipolar transistor (BPT), forward operational mode[2] of SIT (once it was named as BPT mode[6]) corresponds to BPT, however, the height of the pinched-off barrier is lowered by the static induction not through resistor with forward gate voltage, contradicting to the BPT which controls the potential of the base layer through base resistance. Moreover, the storage effect is extremely smaller in SIT than in BPT, because of the very high resistance of the injection controlling point, which is named as intrinsic gate point analogous to intrinsic base. The storage effect in intrinsic gate point is extremely small compared to that in base layer, because of the effectively very thin base as can be imagined as Fig.2. This virtual base structure can be estimated from the V-I character in forward mode shown in Fig.3, which suggests saturation type transistors also can be replaced by SIT.

Inverted SIT Another advantages of SIT are the many possibilities of setting; vertical, inverted or lateral, without lowering the current transport factor, which also makes isolation much easier.

The current from source is squeezed into drain because of the potential barrier formed by the diffusion potential by surrounding gate region. Therefore, inverted SIT usually gives better switching properties because of the smaller drain capacitance and storage effect.

Simplest Manufacturing process for IIL or CMOS[7] Usually IIL or CMOS preparation needs about 8 photo masks, then the preparation is not simple and the yeild is low. This is the main reason why we started from easiest process, which needs only 3 masks

till the configuration of holes for metal contacts. Dimensions of masks used to realize IIL are in the order of μm, even with very easy and simple structure given in the inserted picture in Fig.4, character of the SIT-IIL shows surprising value; $\tau P \geq 2$ fJ, $\tau \geq 5$ ns, and the minimum power supply for operation is 30 pW. Those suggest that even with this primary simple model, SITL has already overwhelmed IIL and CMOS. And limitation for speed comes from storage effect, then, the replacement of BPT by lateral SIT is expected to improve the quality of SITL.

Another possibility, which has already realized as the 4 GHz SIT, is the application of plasma etching technology as shown in Fig.5[8], the oxide or nitride deposited at the bottom is much effective to reduce the storage effect and capacitance. As is easily estimated, the first speciality of the SITL is rather speed than low energy and there are so many structures of logical circuit to be realized. SIT shows much superior character not only when FET is replaced but also BPT is. Also SIT memory (SITM) is expected to have larger future.

(1) J. Nishizawa; International Patents (1971). (2) Y. Watanabe & J. Nishizawa; Japanese Patent (1950). (3) W. Shockley; Proc. IRE, Vol.46, p.1286 (1952). (4) J. Nishizawa et al.; 1972 IEEE IEDM. (5) J. Nishizawa et al.; IEEE Trans. ED, ED-22, p.185 (1975). Y. Mochida, J. Nishizawa & T. Ohmi; to be published. (6) J. Nishizawa & B.M. Wilamowski; Proc. 8th Conf. (1976 International) on Solid State Devices. JJAP, Vol.16 (1977) Supplement 16-1, pp.151-154. (7) J. Nishizawa et al.; 1977 ISSCC p.222. (8) J. Nishizawa et al.; to be published in IEEE trans. on ED.

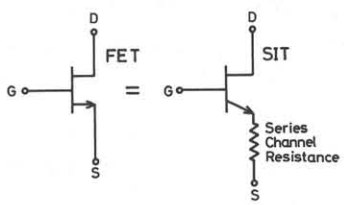

Fig.1 Comparison of FET with SIT.

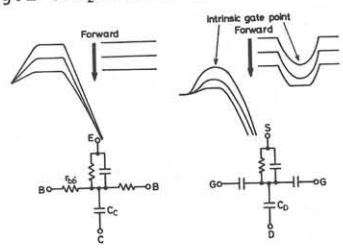

Fig.2 Comparison of BPT with SIT.

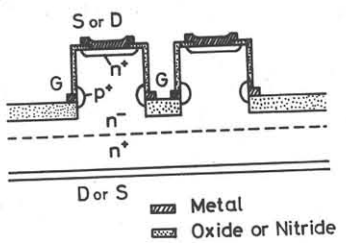

Fig.5. Schematic Diagram of high quality SITL.

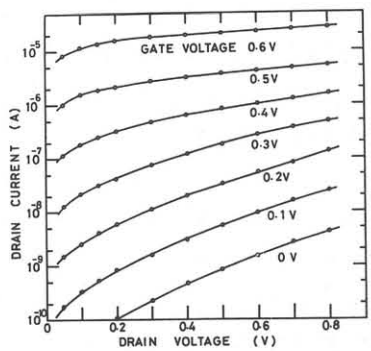

Fig.3 Forward mode operation of SIT.

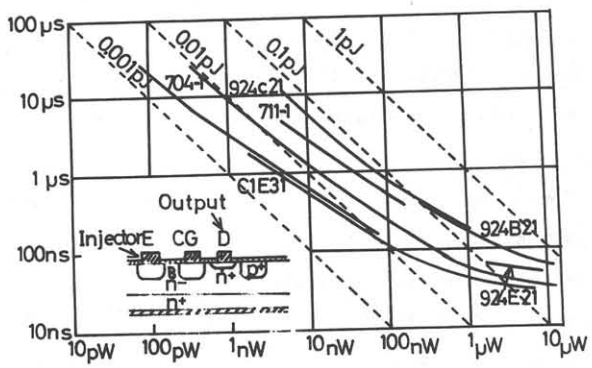

Fig.4 Power-delay diagram