A static induction transistor (SIT) has been proposed as a high power device at high frequency. It has been expected to exceed a bipolar transistor, at high frequency and high power operation, because of its short channels, high voltage operation and negative temperature coefficient of drain current.

An SIT is demonstrated, in this paper, which has output power of above 20 watts at 1 GHz with efficiency of 50%. It is designed to minimize capacitances between electrodes (gate, source and drain) and to obtain large drain current. The cross sectional view of an SIT is shown in Fig. 1.

DESIGN AND FABRICATION

For high frequency operation, high mutual conductance $G_m$ and low capacitances between electrodes $C_{gd}$ and $C_{gs}$ must be attained. For high power operation, high breakdown voltage $B_{V_{gd}}$ and high current level $I_{ds}$ are desirable. These factors depend on resistivity and thickness of the active region. $B_{V_{gd}}$ increases with the resistivity of the active region, while $G_m$ decreases. Both $C_{gd}$ and $I_{ds}$ decrease with the thickness of the active region. In this SIT, resistivity and thickness of the active region were optimized.

Moreover, $C_{gd}$ and $G_m$ depend on the area of the active region. Because $C_{gd}$ is proportional to the area of the active region, and $G_m$ is proportional to source legth (gate width), fine pattern is required to obtain high $G_m$ without increasing the capacitances. In this SIT, fine pattern of 9 μm gate to gate pitch was fabricated by self-aligning technique and by selective plating of gold electrode.

EXPERIMENTAL RESULTS

Typical I-V characteristics of the fabricated SIT are shown in Fig. 2. The drain current of 0.9 A was obtained at applied voltage of 10 V. $G_m$ was 120 - 150 mS and amplification factor $\mu$ was 4 - 5. $C_{gd}$ was about 9 pFs. Breakdown voltage $B_{V_{gd}}$ was 80 volts. From $S$ parameters, the maximum available oscillating frequency $f_{max}$ was estimated to be 3 GHz and maximum available gain $MAG$ at 1 GHz was 5 dB. $S_{11}$ and $S_{22}$ were set near to real axis with lead inductance, as shown in Fig. 3. The power amplification characteristic at 1 GHz is shown in Fig. 4. The maximum output power was 24 watts and the output power was linear up to 20 watts with gain of 4 dB. The drain efficiency was 50%.
CONCLUSION

High power SIT at high frequency, with an output power of 24 watts at 1 GHz, was realized by fine patterning technique using self-aligning and selective gold plating technique and by optimization of the resistivity and thickness of the active region.

ACKNOWLEDGMENT

The authors are grateful to Prof. J. Nishizawa for many helpful discussions. They wish to thank to Dr. K. Shirahata for his encouragement in this work.

REFERENCES