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A TWO PHASE CCD STRUCTURE WITH NARROW-CHANNEL TRANSFER REGIONS

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INTRODUCTION A new electrode structure for two phase CCD is introduced. The built-in directionality is achieved by narrowing the transfer channels of each electrode, effectively producing narrow-channel transfer regions for each storage electrode. The basic performance of this new structure has been evaluated in a 242 element analog delay line with 60 μm channel width and 36 μm element length. Observed inefficiencies per transfer are in the low 10^{-4} for surface channel versions and in the low 10^{-5} for buried channel versions.

PRINCIPLE When the channel width of a FET becomes of the same order of magnitude as the depth of the gate depletion region, an increase of threshold voltage is observed.[1,2] This narrow channel effect has been applied successfully in creating an asymmetrical potential well under an electrode for two phase CCD operations. Figure 1 shows cross sectional views of the electrode structure. For the structure fabricated, each storage electrode has six narrow-channel transfer regions of 4 μm width. In the bottom part of the figure , the cross section of one of the narrow-channel transfer regions is illustrated. The channel stop regions (p^+) surrounding the narrow channel can be formed by self-aligned ion implantation. The actual potential rise of this restricted region with respect to the wide-channel storage region can be controlled by the amount of the ion implantation dose and subsequent annealing conditions. In Figure 2, the actual measured channel potentials are plotted against the gate voltage for the structure fabricated. Both surface and buried channel versions of the device can be built with the same fabrication process, and are compared in the figure.

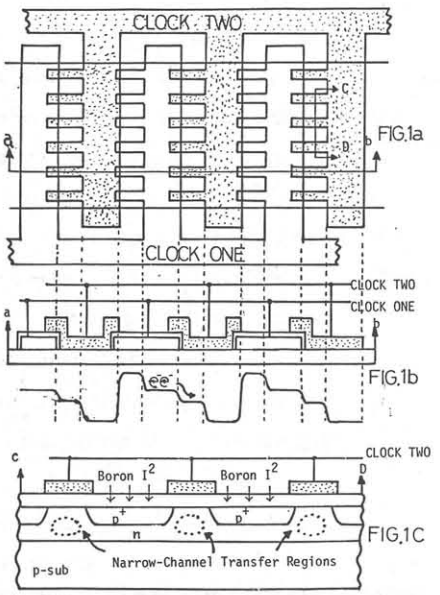

FIG.1 CROSS SECTIONAL VIEWS OF ELECTRODE STRUCTURE

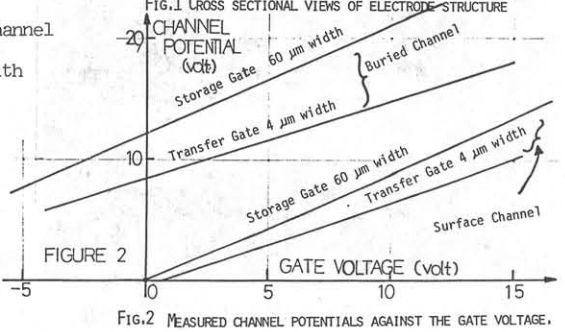

FIG.2 MEASURED CHANNEL POTENTIALS AGAINST THE GATE VOLTAGE.

DEVICE FABRICATION The structure is fabricated on a p-type silicon substrate of a dope level of about 5×10^{14} $cm.^{-3}$ A first level of phosphorus-doped polysilicon is deposited onto an oxidized silicon wafer and defined to form the first set (clock 1) of electrodes. The exposed oxide is then removed and a new gate oxide is thermally grown. Subsequently, the second set (clock 2) of electrodes are formed by the second level of polysilicon deposition. Then, using the polysilicon patternings as an ion implantation mask, boron ions are implanted into the silicon substrate through the exposed portions of the thermally grown oxide. This step provides self-aligned channel stops which surround the narrow-channel transfer part of each electrode. The side-diffusion effect of the implanted boron ions in the subsequent annealing steps works on towards narrowing the actual transfer channel width further down from the value of 4 μm, which was prefixed in the polysilicon electrode definitions. The oxide thickness under the both sets (clock 1 and 2) of electrodes is 0.13 μm, and the ion implantation dose for the buried channel is taken to be 1.5×10^{12} cm^{-2} for the particular device reported in Figure 2.

DEVICE CHARACTERISTICS Both surface channel versions and buried channel versions of the described structure have been built. Figure 3 shows the end sections of a dual 242 element analog delay line with 36 μm element length. The channel lengths of the transfer and storage parts for each electrode are 6 μm and 12 μm respectively. The channel width of the storage part is 60 μm while each storage part is connected to another by six transfer channels of 4 μm width, which are positioned in 10 μm pitch. The input and output wave forms are shown in Figure 4 for a typical device fabricated in buried channel version. The transfer inefficiencies per transfer of less than 5×10^{-4} for surface channel versions and less than 2×10^{-5} for buried channel versions have been measured at element rate of 5 MHz and clock voltage of 12 volt. They are frequency independent up to frequencies corresponding to the limitations imposed by the speed of the free charge transfer.

REFERENCE 1. K.E.Kroell and G.K.Ackermann:"Threshold Voltage of Narrow Channel Field Effect Transistors", SOLID STATE ELECTONICS, 1976.Vol 19, pp.77-81

2. K.O.Jeppson:"Influence of the Channel Width on the Threshold Voltage Modulation in MOSFETs", Electronics Letters. 10th of July 1975 Vol.11,No.14.

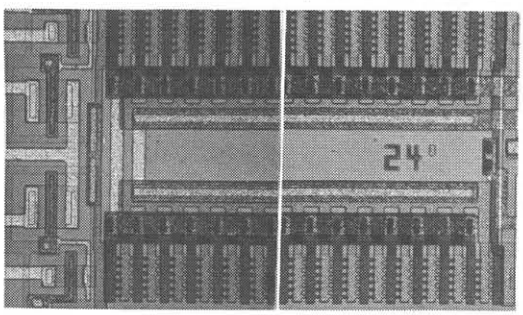

FIG.3 THE END SECTIONS OF A DUAL 242 ELEMENT ANALOG DELAY LINE.

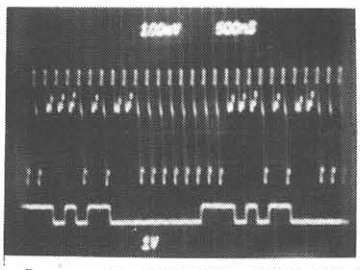

FIG.4 OUTPUT AND INPUT WAVE FORMS FOR A 242 ELEMENT ANALOG DELAY LINE IN BURIED CHANNEL VERSION.