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A—7—2 A NEW MULTI-LEVEL STORAGE STRUCTURE FOR HIGH DENSITY CCD MEMORY

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A 128K-bit CCD memory utilizing a new multi-level storage (MLS) structure has been designed. Using 4 levels of charge, 2 bits can be stored in one storage cell. This structure makes it possible to achieve high packing density without requiring fine patterning. We describe the design of the 128K-bit CCD memory, mainly about the technique of injection and detection of 4 levels of charge.

Fig.1 is a block diagram of the memory chip. The device is organized as randomly addressable 256 shift registers of 512 bits each and as 128K words by 1 bit. Any one register can be selected by the address inputs (A_0, A_1, $\cdots$, and A7), and all registers are serviced by data-transfer clocks (ϕ_1, ϕ_2, ϕ_3, and ϕ_4) and mode control clocks such as read and write (R/W), chip select (CS) and column address strobe ($\overline{CAS}$).

The writing operation to store 2 bits into one storage cell is illustrated in Fig.2 which shows input electrodes, surface potential under the electrodes and the timing diagram of internally generated clocks, ϕ_T, M, and S. The first signal, "1" or "0", is injected into the S input cell at time B (Fig.2) following a low-to-high transition of the clocks. The first signal is sampled when the clock M returns to the low level (time C), and during the interval C-F it is stored in the S input cell. The second signal, "1" or "0", is injected into the I input cell at time E, which is electrically separated from the S input cell. The second signal is sampled when the clock ϕ_T returns to the low level and the excess charge is swept out to the input node. During the interval F-G,the signal charge packets in the S and I input cells are mixed and divided again when the clock M goes low. The S electrode has twice as large area as the I electrode, so that the charge level stored in the S input cell is a combination of the first signal and the second one. As the result, the charge level of the S input cell is one of 1, 2/3, 1/3, and 0 in the unit of full charge as is listed in Table 1.

For read and refresh operations, a high performance cross-coupled sense amplifier is used to detect the charge. The output signal charge which contains 2 bits of data is dumped onto the output node at time A (Fig.2). The level of this output node is compared twice with the different reference levels each time to detect 2 bits of the stored data successively. The detection of the first signal can be achieved by comparing the output signal charge with 1/2 level of full charge generated from the dummy register. After the detection of the first sig-

nal, the new 1/6 or 5/6 level is set which is determined by "0" or "1" of the first signal. Using this new level, the second signal can be detected in the same manner as the first one.

The process is an extension of n-channel Si-gate technology. A double level polysilicon gate structure is used within the CCD array. Memory cell size is 208 μ^2/bit.

Fig.1 Block diagram of the 128K-bit CCD memory

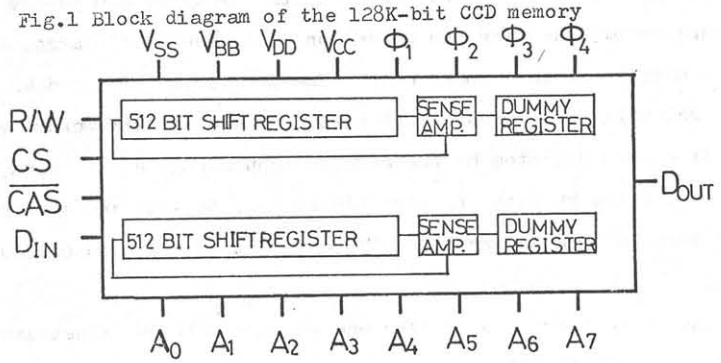
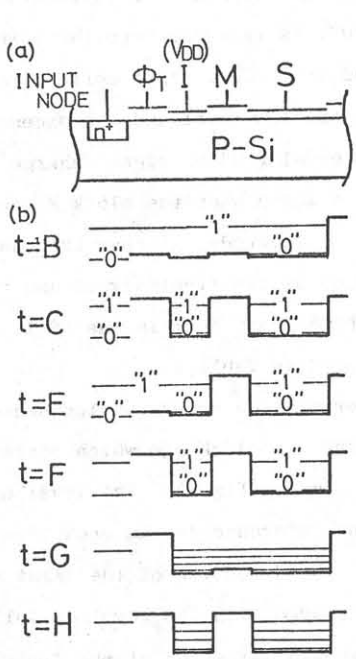


Fig.2 (a) Cross section of the input stage (b) Surface potential along the cross section (c)Timing diagram



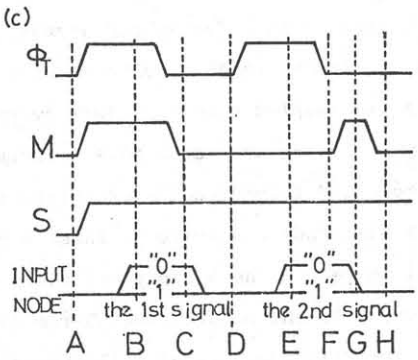


Table 1 Stored charge level in the unit of full charge

the 1st signal	the 2nd signal	stored charge level
1	1	1
1	0	2/3
0	1	1/3
0	0	0