A—7—4   High Power Gate Turn-Off Thyristors

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High power gate turn-off tyristor (GTO) development is one of the recent topics in the field of power electronics, because of the remarkable merit wherein forced commutation is not required for inverter and chopper applications. In several previous publications on high power GTO's, maximum gate turn-off currents (I_{ATO}) in the 50 to 200 Ampere range have been reported.[1],[2] This paper describes design considerations for increasing I_{ATO} beyond the above values, as well as the results of characterization carried out on the developed device units.

Figure 1 shows the schematic configuration of a mesa-type GTO-segment, including impurity doping profiles and other design parameters. An actual GTO-unit consists of a plurality of the segments, which are parallel-connected to each other.

As a result of numerous experimental fabrications and characterizations, the mask pattern shown in Fig. 2 was determined. It consists of 260 emitter fingers 4 mm in length and 300 microns in width.

Figure 3 shows an example of the waveforms during the gate turn-off transient. Operational turn-off gain, defined as ($I_A/I_{G,peak}$), is around 4. This value depends upon gate current rising rate (dI_G/dt), which is 30A/µs in this example. Anode voltage rising rate (dV_A/dt) is suppressed by the snubber circuit to an appropriate value, in order to decrease the switching loss.

Figure 4 shows experimental I_{ATO} vs. (V_{J1}/ρ_{SPB}) characteristics with n-base resistivity ρ_{NB} as a parameter, where V_{J1} stands for the gate-cathode breakdown voltage, and ρ_{SPB} stands for the p-base layer sheet resistance. Theoretical
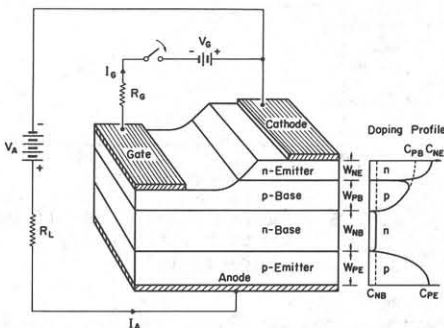

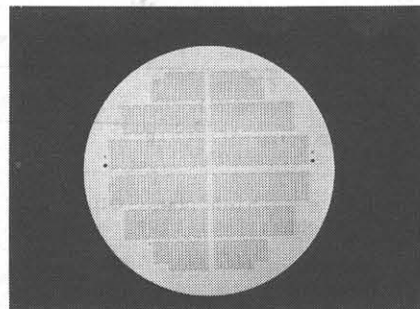Fig. 1   GTO-segment configuration

Fig. 2   Mask pattern for GTO-unit

estimation of V_{J1} can be made on assumptions of the Gaussian doping profile and the linearly-graded p-n junction[3], while ρ_{SPB} can be calculated as a function of the doping profile and the carrier mobility. As is shown in the figure, I_{ATO} can be increased by increasing (V_{J1}/ρ_{SPB}). This fact is similar to one obtained by Wolley.[4] Another way of increasing I_{ATO} is to increase ρ_{NB}, which is, to our knowledge, a new result. By making (V_{J1}/ρ_{SPB}) sufficiently high, excess carriers are efficiently removed from the p-base, thus resulting in a high I_{ATO}. It is assumed that the dependence on ρ_{NB} is due to a wide depletion layer formation during the turn-off process. Main characteristics for the fabricated devices are given in Table 1.

Another group of test samples were fabricated for I_{ATO} vs. frequency characteristics evaluation. Figure 5 shows a result for the 3 Ohms load resistance, 30 percent duty.
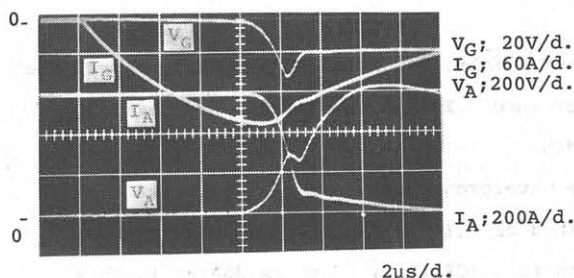

V_G; 20V/d.
I_G; 60A/d.
V_A; 200V/d.

I_A; 200A/d.

2µs/d.

Fig. 3   Gate turn-off waveforms

Fig. 4   Maximum gate turn-off currents vs. (V_{J1}/ρ_{SPB}) characteristics with n-base resistivity as a parameter.

Forward blocking voltage (Tj=115°C)	1300V
Maximum gate turn-off current(Tj=110°C)	600A
On-state voltage(I_A=600A)	1.5V
Surge on-state current (50Hz, sinusoidal one-cycle peak)	3500A
Latching-Holding current	2A
Gate turn-on time	10µs
Gate turn-off time (Tj=110°C, I_A=600A)	12µs
Operation turn-off gain (Tj=110°C, I_A=600A)	4

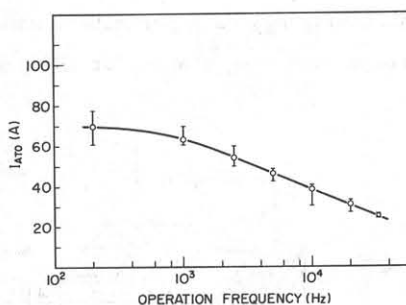Table 1   Main high power GTO characteristics

Fig. 5   Maximum gate turn-off currents vs. frequency characteristics

REFERENCES
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4. E.D. Wolley, IEEE Trans., Electron Devices vol. ED-13, pp.590-597, July 1966