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Merging Technologies: Bipolar and MOS

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Trends in advanced process and device technologies in bipolar and MOS integrated circuits are observed to force a blurring of traditional boundaries between these two historically different technologies. In earlier times MOS workers employed (often) radically different approaches to device and process design for MOS integrated circuits and devices when compared to bipolar workers. However, with the advancement of technology led by prime motivations of new families of VLSI MOS circuits for sub-nanosecond logic applications we find that techniques and processes known primarily to but one of these major disciplines are essential to the continued evolvement of the other discipline.

In this review paper we discuss these technology mergings particularly as related to sub-nanosecond logic integrated families. Particular attention is focused upon DMOS, VMOS, DVMOS, and Si-MESFET logic families and their associated process designs. Process considerations relative to buried diffusion and epitaxial growth, tight geometry control with minimum dimension lithography, surface state control, shallow junction technologies for reduced parasitics, and ion implantation are all discussed.

Finally a process modeling technique is described that is (basically) technology insensitive and its use described for modeling of new generation MOS/LSI with regards to impurity profile considerations.

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