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# B—3—2 MECHANISM OF INHERENT MEMORY IN THIN FILM EL DEVICE

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Existence of inherent memory in a thin film multilayered EL device was observed[1)] and developed by virtue of hysteresis loop measured in Voltage - Brightness characteristics as shown in Fig.1. Fig.2 shows the basic construction of the EL device which consists of ZnS:Mn EL layer sandwiched by $Y_2O_3$ insulating layers. Under certain constant ac sustain voltage, $V_s$ in Fig.1, switching or writing from low brightness state to any intermediate high brightness state is realized by instantaneous excitation of a higher voltage pulse or UV light irradiation[2)]. A series of experimental studies were carried out on the electrical and optical properties of the EL device and on a single ZnS thin film for the clarification of memory mechanism.

## Experimental Results

Photo.1 shows a typical Charge-Voltage characteristics of a three layered EL device measured by a Sawyer-Tower circuit. The amount of charge Q on the electrode of the EL device at zero voltage facilitates computation of the charge stored at the boundary region between the insulator and AnS layer by means of Poisson's equation. Calculated values of the charge at various ac peak voltage, together with the brightness observed at respective voltages, are shown in Fig.3. Fig.4 shows the way in which the memory is affected by the thickness of ZnS layer. Measurement of Voltage-Brightness characteristics is carried out under various temperature as shown in Fig.5. Memory width is defined as the voltage width on a hysteresis loop at a brightness of 10 nit. Fig.6 shows the relation between the memory width and the temperature at which the device is operated. Fig.7 shows the thermally stimulated current (T.S.C.) of ZnS:Mn EL layer. The energy of the trapping level is calculated to be about 0.8 eV below the conduction band based upon the temperature at which the peak thermally stimulated current $I_p$ occurs. The captured electron density still remaining at the trap level at each temperature may be estimated by integrating the area underneath the T.S.C. curve from the higher temperature side. The result is shown as $N_t$ in Fig.6, which is very similar to the temperature dependence of memory width $V_w$.

## Discussion

This memory effect is observed in the three layered EL device, but it is not found in the single layered nor in the double layered EL device. Furthermore, high brightness electroluminescence and inherent memory are realized only under ac voltage excitation. Mobile electrons within the ZnS layer displace toward the boundary region and stay there forced by the external electric field, thus forming an internal polarization. When the external field alternates' the internal polarized field adds up with the external field, resulting in an enhanced emission of light. Therefore, even at the same ac peak sustain voltage, the difference of polarized charge results in different brightness of light, which accounts for the hysteresis effect observed in the Voltage - Brightness characteristics. Polarization charge is thought to be originated from deep traps whose level exist at about 0.8 eV below conduction band as calculated in the measurement of T.S.C.. Under high electric field of 1 - 2 x $10^6$ v/cm, captured electrons at deep trap can be released by field effect and/or collision with primary electrons. Electrons thus released contribute to exciting the Mn centers[3]. The increase of the peak value of the ac applied voltage causes the number of electrons that are released from the trap level to grow. These electrons move back and forth between the boundaries. Further increase of voltage releases most of the electrons from the deep trap, hence, leveling off of brightness results. In the decreasing cycle of the ac voltage, the recombination probability into deep traps remaind to be low at high electron velocity, which accounts for the cause of hysteresis effect in brightness versus voltage characteristics. The results of temperature dependence and thickness dependence upon memory may be explained from the proposed model as mentioned above.


References

1) M. Takeda et al.: Proc. 6th Conf. Solid State Devices (1974) 103.
2) C. Suzuki et al.: 1977 SID International Symposium § 8.3.
3) S. Tanaka et al.: J. Appl. Phys. 47 (1976) 5391.


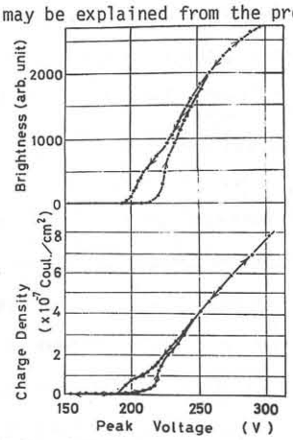

Fig.3 V-B and V-Q characteristics.

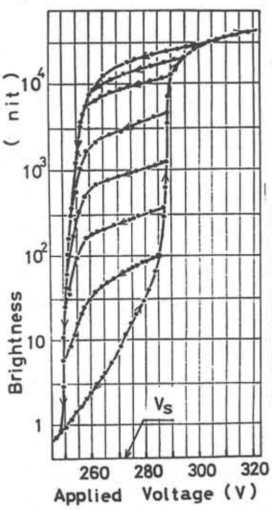

Fig.1 V-B characteristics.

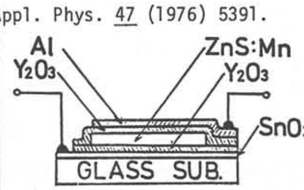

Fig.2 Sample construction.

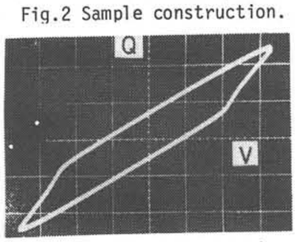

Photo.1 V-Q characteristics.

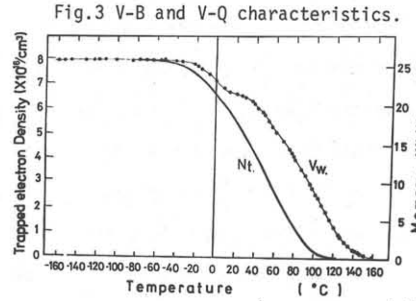

Fig.6 Temperature dependence of $N_t$ and $V_W$.

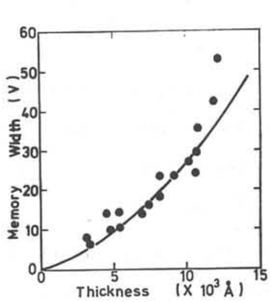

Fig.4 Thickness dependence of memory width.

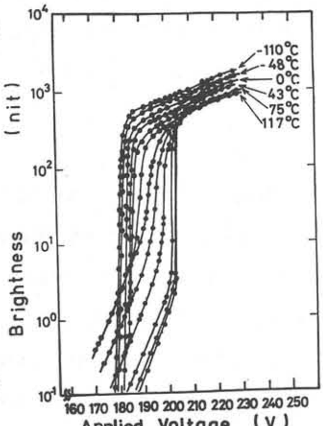

Fig.5 Temperature dependence of V-B characteristics.

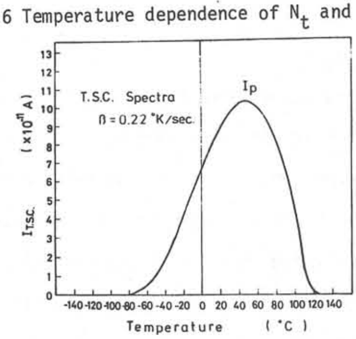

Fig.7 T.S.C. spectra.