C—1—2 X-and Ku-band Performance of Submicron Gate GaAs Power FETs

Y. Aono, A. Higashisaka, T. Ogawa and F. Hasegawa

Central Research Laboratories, Nippon Electric Co. Ltd.,

Miyazakidai, Kawasaki, Japan.

After realizing eminent performance of C-band GaAs power FETs, demands for the development of X-band or Ku-band GaAs power FETs are increasing. In order to obtain an adequate power gain at these frequencies, it is inevitable to reduce the gate length of the device. Furthermore, the fabrication process should be productive for practical purposes.

We have developed X-band GaAs power FETs with a submicron gate and with a cross over structure, by applying the technologies which have been successfully used for our prominent half micron gate low noise GaAs FETs (NE 388). The developed device delivered 1.0W saturated power at 11GHz with a linear gain of 5.5 dB and with a power added efficiency of 18.5%. At 13.6 GHz, a saturated output of 0.63W with a linear gain of 4.5 dB was obtained.

Figure 1 shows the pattern of the developed GaAs FET. It has one chip two cell structure, each cell having 10 gate fingers with 75 μm gate width. The total gate width of one chip two cell device is 1500 μm. The pattern is also designed so that a chip with four cells (3000 μm gate width) can be cut out. The gate length is about 0.5 μm and the source to drain spacing is 4 μm.

The gate finger length was determined by estimating the transmission loss at the gate-source transmission line. It is designed that the power loss is less than 6% of the total output power. The gate to gate spacing was adopted to be 20 μm from the thermal resistance of the device so that the temperature rise is less than 60°C.

The carrier density of the active layer is about $1 \times 10^{17} cm^{-3}$. The developed one chip device (1500 μm gate) normally gave pinch off voltages of 4.5∿5.5 V, drain saturation currents of 340∿400 mA and transconductances of 80∿88 mU.

Figure 2 shows the output power P_{out}, drain bias current I_{ds} and the gate current I_G of the two cell device (1500 μm gate) at 11 GHz, against the input power level P_{in}. As the gate bias is increased, the power added efficiency increases and the linear gain decreases, and the saturated output power was maximum at the gate bias of -3.0 V. The output power seems to saturate at the input power

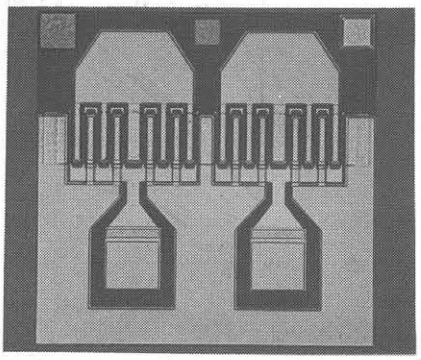

Fig.1.Photograph of the device pattern.

level where the gate current begins to flow, indicating that the r.f. swing is no more sinusoidal at this point. The drain bias current is also affected by the deformation of r.f. swing.

The output power could be increased by increasing the drain bias voltage and the number of cells. Figure 3 shows the output powers of a 3000 μm gate device at 11 GHz for different bias voltages. The output power of 1.0 W was obtained with a power added efficiency of 18.5%. The drain bias voltage was 12 V. The linear power gain was 5.5 dB in this case, but it could be increased to 7.5 dB by tuning at a lower input power level.

The performance at 13.6 GHz is shown in Fig. 4. The maximum output power of 0.43 W is obtained for a 1500 μm gate device and 0.65 W for a 3000 μm gate device. The linear gains are 4.5 dB for both devices.

It has been shown here that the GaAs power MESFETs with a submicron length gate can give a reasonable output power and gain for practical purposes at X-and Ku-band.

The authors would like to express their thanks to Mr. Aihara for the performance measurements at 13.6 GHz, and to Messrs. Y. Kaneko and K. Noguchi for the growth of the epitaxial wafers

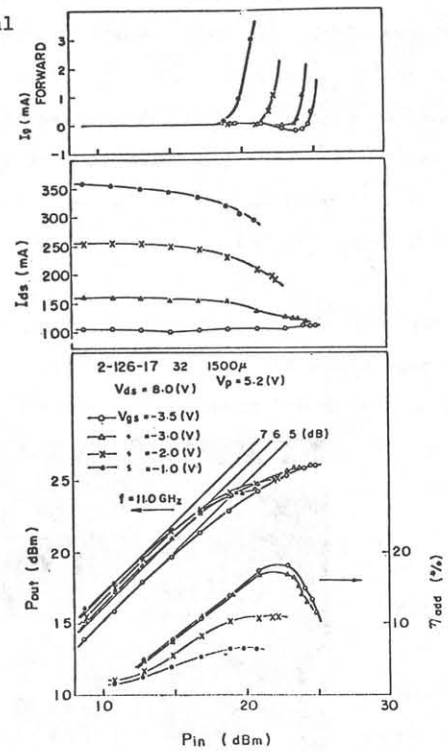

Fig. 2, Gate bias dependence of output power, gate and drain currents.

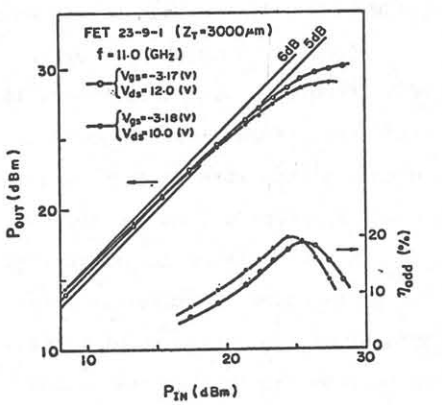

Fig. 3, Output power and power added efficiency at 11 GHz

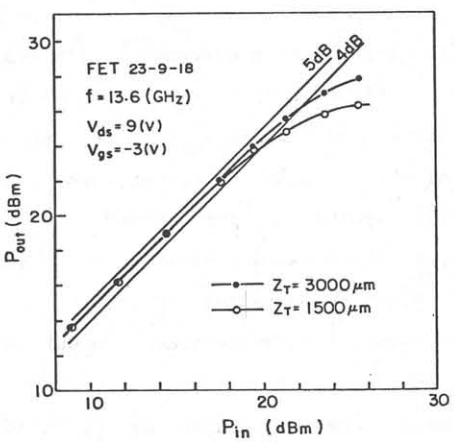

Fig. 4, Output power at 13.6 GHz.