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(Invited)

A VMOS 16K-BIT EPROM

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A 16K-Bit Electrically Programmable Read Only Memory (EPROM) has been developed using the VMOS technology[1]. The EPROM is fabricated with a variation of the standard VMOS process[2] with the addition of a polysilicon layer for the floating gate, a p-type implant to provide programmability, and a depletion transistor implant which replaces the normal resistor implant. The process provides planar enhancement and depletion transistors, a VMOS transistor, and the VMOS EPROM transistor.

The memory cell consists of a VMOS transistor at the intersection of a polysilicon word line and the diffused bit line. The cell contains no contacts or top side ground interconnect and is 15 x $15\mu^2$ using 5 micron rules.

The circuit program voltage is 15 volts and the program time per word is less than 50 ms. Erasing the data is by ultra violet light and is accomplished in less than 10 minutes.

The VMOS EPROM is organized 2,048 words by 8 bits wide.

A photomicrograph of the chip is shown in Figure 1. The X-decode and word line drivers are situated in the middle of the memory array and dissipate no power during the power down mode of operation. In the read mode of operation the circuit requires only a single 5 volt supply. The circuit is fully static in both the read and program mode of operation. The input-output buffers are located at the left of the chip and sink 8 mA at 0.4v and source 4.5 mA at 2.4v with V_{CC}=4.5v. The chip area is 18,600 mil^2 (121 x 154 mil^2).

The room temperature test results of the VMOS EPROM are:

T_{ACC}	250 ns, V_{CC} = 4.5v
I_{CC}	31 mA, V_{CC} = 5.5v
I_{CC}(Power Down)	13 mA, V_{CC} = 5.5v
I_{pp}(Program)	10.5 mA, V_{pp} =15v

[1] D.A. Draper, J.J. Barnes, and F.B. Jenne', "Fabrication and Characterization of a VMOS EPROM", IEDM Digest Tech. Papers, pp. 277-283, December, 1977.

[2] T.J. Rodgers, W.R. Hiltpold, B. Frederick, J.J. Barnes, F.B. Jenne', and J.D. Trotter, "VMOS Memory Technology", IEEE J. of Solid-State Circuits, Vol. SC-12, No. 5, pp. 515-524, October, 1977.

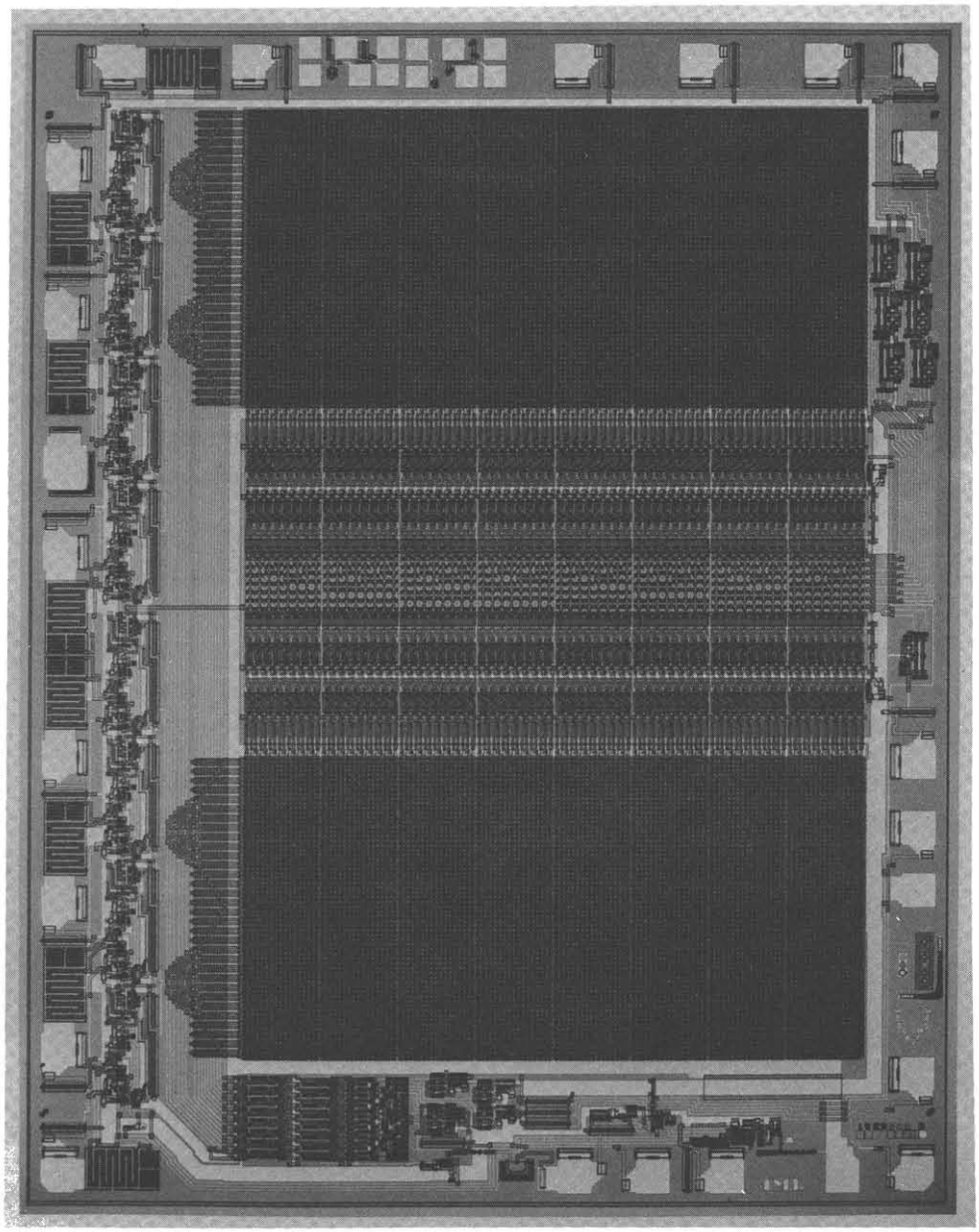

Figure 1. Photomicrograph of the VMOS
16K-Bit EPROM chip