A－1－2 N-channel Si-gate MNOS Device for High Speed EAROM

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In recent years, MNOS devices have been the subject of extensive research.[1)2)] The tangible result has been that several electrically alterable nonvolatile memory have appeared on the market.[3)] However, all of these MNOS memory LSI's are p-channel Al-gate type and retain read cycle limitations owing to the cell structure. Their read access time is greater than 650 ns and their fabrication process is no longer compatible with advanced LSI technology. The purpose of this work is to develop an n-channel MNOS device which has no read cycle limitations as well as to develop a new Si-gate fabrication technology which produces high speed EA memory LSI's.

Our memory cell consists of two transistors per bit, i.e. a Si-gate MNOS memory transistor and a Si-gate enhancement mode switching transistor. This configuration frees our device from read cycle limitations. The cross section of the cell is shown in Fig. 1. The MNOS gate is a layered structure of 2.0nm thick tunnellable SiO_2, 50nm Si_3N_4 and 0.3 μm poly Si.

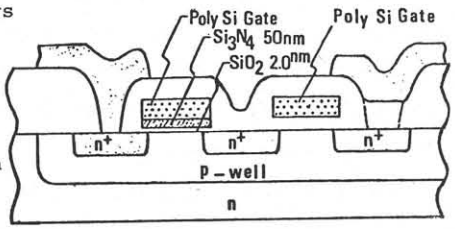

Fig 1 Cross Section of The Memory Cell

An outline of processing steps is as follows: The starting Si wafer is n-type (100), not epitaxial; a memory part and peripheral MOS circuits are formed in each p-type well; MOS gates are prepared by patterning the first poly Si layer; then in the memory part, thin SiO_2, Si_3N_4 and the 2nd poly Si layers are successively formed and patterned to make MNOS gates; finally, the N^+ layer is prepared by self aligned phosphor implantation.

In conventional Al-gate MNOS's, a thick SiO_2 layer has been widely used near the source and/or drain junctions. These so called dualgate or trigate devices, are equivalent to the serially connected common gate memory and non-memory transistors. When read addressing, a certain gate bias higher than Vth of the memory part is applied to the common gate and unwilling weak writing occurs in the memory part.

In the Si-gate MNOS transistor no thick SiO_2 is used, permitting a large Vth window. The Vth_W (write state) is $\geq$2 volts and Vth_E (erase state) is $\leq$-3 volts, at initial write or erase conditions. At read out, addressed gate of the switching MOS transistor is V_{DD} (5 volts), whereas the MNOS gate is still 0 volts. Consequently, unwilling weak writing during read out does not take place thereby eliminating read cycle limitations.

In the device, anomalous positive Vth shift caused by applying negative gate voltage[4)] which results in the instability of poly Si-Si_3N_4 interface is not observed.

The Si-gate self aligned structure facilitates a memory cell smaller than conventional Al-gate dual or trigate devices. The memory cell of our test devices was

further reduced to 17.5x17 μm^2 by 4μ technology.

Retentivity is the most important characteristics of MNOS memory LSI's. The Vth change for the device stored under various conditions is shown in Fig.2. The decay rate $M=\partial Vth/\partial \log_{10} t$ at room temperature storage after 10^4 rewrite cycles is 0.2. Even at 125°C, M is about 0.2 for Vth_E(<0) and 0.45 for Vth_W(>0). From the results, a 10-year unpowered data storage capability has been confirmed at 125°C, with further nonvolatility testing now in progress.

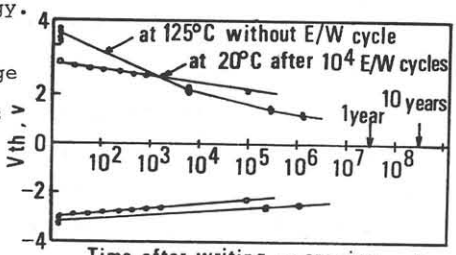

Fig 2 Retention characteristics

The dependence of write and erase characteristics on the thin SiO_2 thichness are shown in Fig.3. With 2.0 nm SiO_2 devices, pulse width necessary for writing is 100 μs and erasing is 3ms. Test devices containing a memory array with addressing and I/O circuits have been fabricated. The device can be operated by a single 5-volt power supply,thus, a read access time of less than 200 ns has been measured.

The Si-gate MNOS device is compared to a conventional Al-gate MNOS in Table 1.

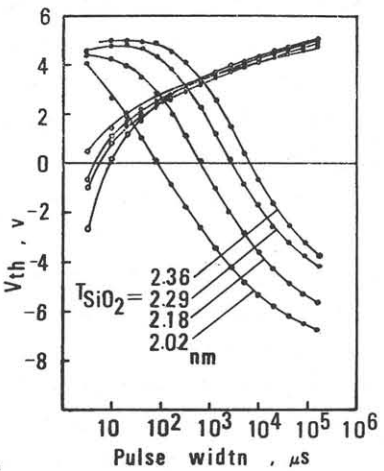

Fig 3 Erase and write characteristics

Conclusions The main features of our EA memory devices are summarized as follows:

[1] An n-channel MNOS device is proposed which can be prepared by a Si-gate self aligned process together with Si-gate E/D MOS transistors for the peripheral circuit.

[2] By using a two transistor (MNOS+switching MOS) per bit configuration, read cycle limitation is removed. The cell size is smaller than conventional Al-gate MNOS devices.

[3] The memory device has high speed programming characteristics; write time is about 100μs and erase time is less than several ms. A 10-year nonvolatility is confirmed in unpowered condition at 125°C.

[4] Read access time of less than 200 ns has been obtained by a single 5-volt power supply.

[5] The application of this technology should realize large scale EAROM and EA memory on chip devices in the near future.

Table 1 COMPARISON OF MNOS DEVICES

PROCESS	P-CH. Al-GATE	N-CH. Si-GATE
POWER SUPPLY (READING CYCLES)	-10 V	+5 V
ACCESS TIME (TYPICAL)	650 ns (CLOCK INTERFACE)	200 ns (FULLY STATIC)
DEVICE / BIT	1 or 2	2
CELL SIZE	650 μm^2	300 μm^2
READ CYCLE LIMITATION	$10^{6\sim11}$	NO LIMITATIONS

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4) P. C. Y. Chen, IEEE, Trans. ED-24, 584 (1977).