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A−1−3 Suppression of Anomalous Drain Current in Short Channel MOSFET

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Increasing sensitivity of MOSFET characteristics to two-dimensional geometry, as a consequence of the scaling-down approach,[1] essentially gives rise to several problems such as difficulty in controlling the threshold voltage and the current voltage characteristics. This paper describes two-dimensional analysis of the scaled-down MOSFET with deep ion implantation into channel region to reveal a role of the ion implanted layer on suppression of the broadening of Log I_D- V_G slope and anomalous excess drain current in the subthreshold region as well as modification of the short channel effects in threshold voltage, and, finally, derives optimum condition for the ion implantation which can allow us larger tolerance in designing very short channel MOSFET.

Schematic cross section of the n-channel MOSFET is shown in Fig.1, where N_{SUB}, N_{SF1} and N_{SF2} are the accepter impurity concentrations in the layers, respectively. X_1, X_2 and X_J are the thicknesses of the two doped layers and the junction depth, respectively. T_{OX} is the gate thickness, and L_{EFF} the channel length. V_{DD}, V_{BB} and V_G are the drain voltage, the back gate bias and the gate voltage, respectively. Two basic equations, Poisson's equation and the current continuity equation, were numerically solved[2] by means of Stone's iterative method.

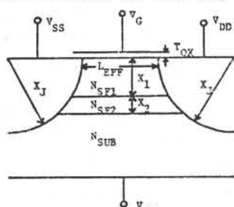

Fig.1. Cross section of MOSFET.

Fig.2 shows some examples of calculation in comparison with experimental results, which demonstrates excellent agreement. Fig.3 shows typical examples of calculated I_D - V_G characteristics for various effective channel lengthes with and without deep channel ion implantation. We should note that broadening of a slope in the subthreshold region and excess drain current become more significant with decreasing channel length. It is very clear that both amount of the excess drain current and the slope of Log I_D - V_G characteristics are drasticly improved in case of the ion implanted device with L_{EFF} of

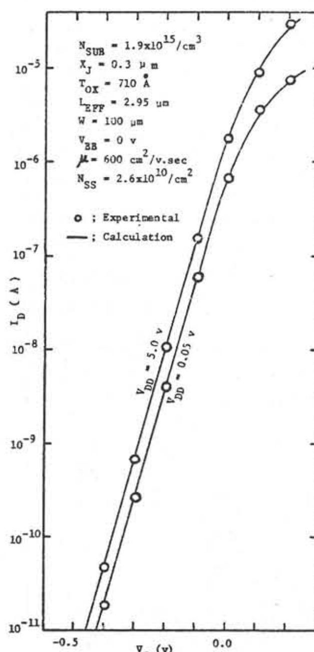

Fig.2. Experimental and calculation log I_D vs V_G with V_{DD} as a parameter for a uniform substrate impurity profile.

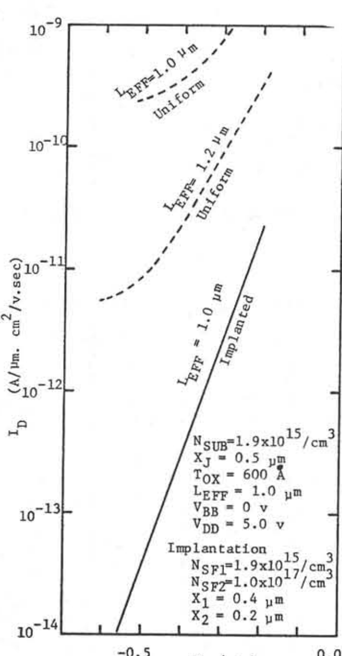

Fig.3. Calculated log I_D vs V_G of a uniform and an implanted MOSFET.

even as small as 1.0 μm. The remainder of the paper will be dedicated to how to interprete the role of ion implanted layer and how to optimize the ion implantation for designing very short channel MOSFET and VLSI. Potential distributions in several MOSFETs are shown in Fig.4. Note that the potential for L_{EFF}=1 μm stays at relatively high level until 1.0 to 1.2 μm in-depth, while the one for longer L_{EFF} drops down quickly with increasing thickness. The ion implanted device with L_{EFF} = 1 μm behaves as if it had relatively longer channel length. Thus, the anomalous drain current which is due to a punch-through current in deeper region, shoud be effectively suppressed by the deep-ion implantation of accepter impurity as well as the slope of Log I_D - V_G characteristics. The slope of Log I_D - V_G characteristics in the subthreshold region is calculated as a function of the depth of ion implanted layer for various concentrations of N_{SF2}, and plotted in Fig.5. Combinations for N_{SF2} and the depth X_1 show certain optima for minimizing the inverse slope n as clearly seen in the figure. Since electron current becomes strongly localized along the surface with increasing back gate bias, the effect of ion implantation on the slope and the excess drain current tends to be less sensitive in comparisn with the zero back gate bias. From Fig.5 and behaviors of anomalous drain current, one can obtain optimum areas surrounded by several X_1 - N_{SF2} curves as described in Fig.6. Consequently, both slope of Log I_D - V_G characteristics and additionaldrain current in the subthreshold region can be significantly improved by choosing appropriate combinations for dose and projected range for ion implantation of accepters into channel region.

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References

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(2) M.S. Mock : Solid State Electronics, 16 (1973) 601.

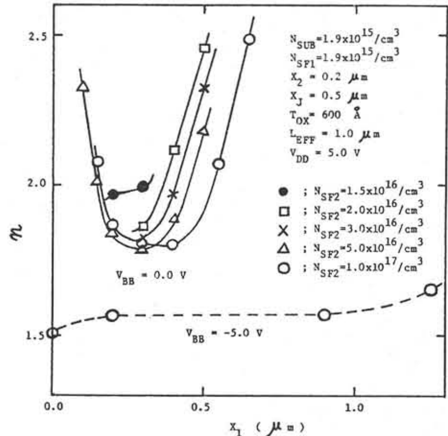

Fig.5. n($\equiv$q.dV_G/kT.dlog I_D) vs X_1 for various V_{BB} and N_{SF2}.

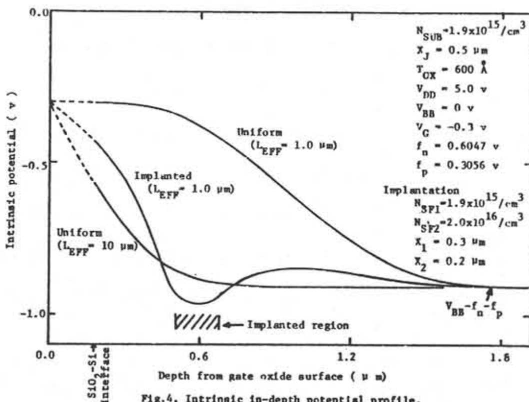

Fig.4. Intrinsic in-depth potential profile.

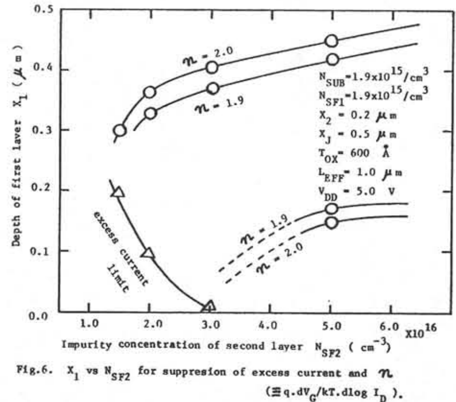

Fig.6. X_1 vs N_{SF2} for suppresion of excess current and n ($\equiv$q.dV_G/kT.dlog I_D).