

A-1-4 Novel High Density, Stacked Capacitor MOS RAM

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A novel one transistor type MOS RAM cell has been successfully developed to achieve a higher degree of integration than realized to date with conventional RAMs. This cell provides a remarkable area reduction and/or an increase of storage capacitance by stacking the main part of the storage capacitor on the address transistor and is called the stacked capacitor (STC) cell. The cross section and plane views of a 2 bit STC cell are shown in Fig.1 (a) and (b) respectively. This STC cell has a triple level poly-Si structure which consists of poly-Si word lines and metal (Al) bit lines. That is, each address transistor gate electrode is composed of the first poly-Si layer and each stacked capacitor is composed of the second poly-Si layer,  $\text{Si}_3\text{N}_4$  film and the third poly-Si layer.

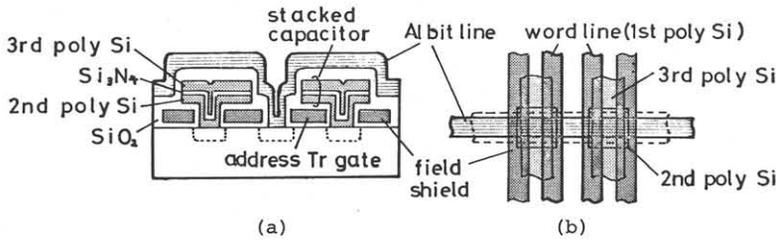


Fig.1 STC cell. (a)cross section view. (b)plane view.

Two new techniques were developed to fabricate the STC MOS RAM. These are : (1) self-aligned contact, and (2) self-aligned etching of the capacitor electrodes. The new self-aligned contact technique is based on selective oxide coating of poly-Si electrodes which utilizes the impurity concentration dependent oxidation of Si.<sup>1)</sup> The second poly-Si electrode of the stacked capacitor is located above the address transistor gate electrode and contacts the address transistor drain or source without registration tolerance using the self-aligned contact technique. The second and the third poly-Si electrodes of the stacked capacitor are formed simultaneously with the same photoresist pattern by the self-aligned etching technique. Therefore, effective storage capacitance is not reduced due to the registration tolerance.

The figure of merit, the  $C_s/C_d$  ratio versus cell area  $A_c$  relation, is shown in Fig.2 in comparison with a conventional cell with a double

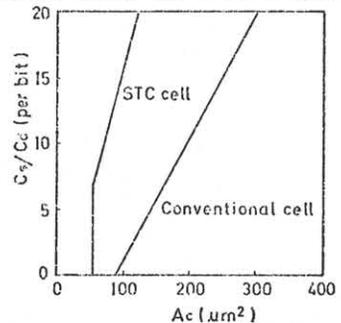


Fig.2  $C_s/C_d$  ratio vs cell area  $A_c$  relation.

level poly-Si structure. Here,  $C_s$  is the storage capacitance and  $C_d$ , the stray capacitance of a bit line. The  $C_s/C_d$  ratio is remarkably larger in STC cells than in conventional cells. Therefore, the output signal is larger in STC cells.

A photograph of a 256 bit STC MOS RAM cell and a conventional cell with 3  $\mu\text{m}$  technology are presented in Fig.3 (a) and (b) respectively. It is evident that the STC cell area is approximately one third of the conventional cell area. A scanning electron micrograph of the STC cell cross section is shown in Fig.4. Here, the stacked capacitor structure is clearly seen.

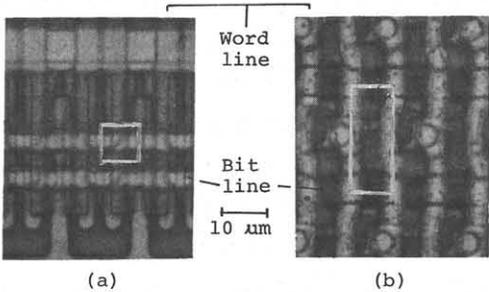


Fig.3 Photograph of memory cell.  
 (a) 256 bit STC RAM cell.  
 (b) conventional cell.

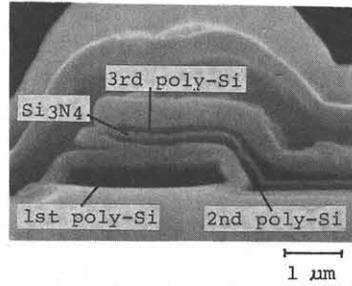


Fig.4 Scanning electron micrograph of 256 bit STC RAM cell cross section.

The input and output pulse waveforms of the 256 bit STC MOS RAM are shown in Fig.5. The STC MOS RAM operated successfully even where the pulse timing was not optimized. The charge stored time normally ranged 0.1 sec to 1 sec at room temperature.

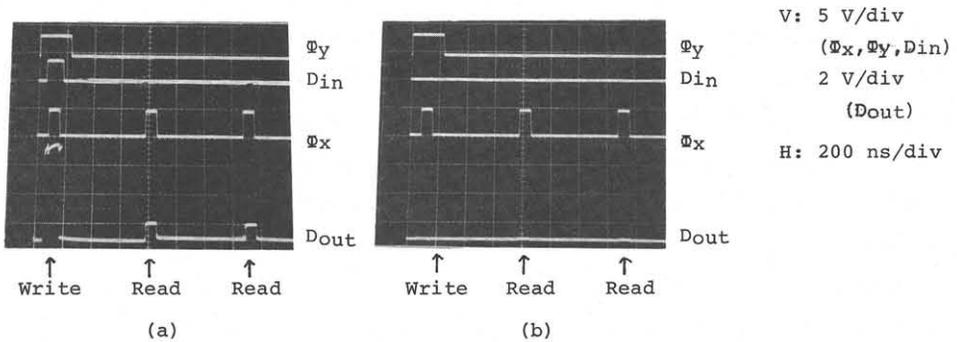


Fig.5 Input and output pulse waveforms of 256 bit STC MOS RAM.  
 (a) High write and read. (b) Low write and read.

As mentioned above, the STC MOS RAM can bring a higher degree of integration to MOS RAMs. On the other hand, a demerit of the STC MOS RAM is that the fabrication process is somewhat complicated comparing with conventional double level poly-Si processes. However, fabrication could become more feasible by modifying part of the STC MOS RAM processes.

Reference: 1). H. Sunami and M. Koyanagi, SSD77/26 (1977)