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An Isolation Structure and Layout of The Buried Oxide CMOS-IC

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The Buried Oxide (BO) MOS device is expected to possess the SOS-MOS performance without SOS in speed and density particularly to CMOS-IC, because it has the distinct isolation feature in integrated circuits. It has been reported that the important differences from SOS-MOS in characteristics are no degradation of channel mobilities nor abnormal junction-leakage and no kinks on I-V curves because of the channel region being common to the substrate just as the conventional bulk MOS-IC. Thus it has been pointed out that the most attractive application of this unique isolation technique may be high-density CMOS-IC's (1),(2).

A constant nightmare for design engineers on the conventional high-density CMOS-IC is the latch-up problem or a parasitic PNPN device. The latch-up phenomena in CMOS circuits triggered by surge voltage on the power supply line are essentially the voltage-trigger turn-on of a four-layer Shockley diode (3) with shorted-emitter structures. An equivalent circuit is shown in Fig.1. The latch-up voltage now can correspond to the break-over voltage V_{BO} of the diode (4), which is given by:

$$V_{BO} = V_{BD2}\left[1 - \alpha_N\left(1 - \frac{1}{1 + \frac{qR_N I_{S1}}{kT}}\right) - \alpha_P\left(1 - \frac{1}{1 + \frac{qR_P I_{S3}}{kT}}\right)\right]^{1/3}$$

where V_{BD} and I_S are the break-down voltage and the saturation current of corresponding junction, α and R are the current gain and base resistance of corresponding PNP and NPN transistors, q, k, and T are the electronic charge, Boltzmann constant, and absolute temperature respectively. The rule of thumb for the design engineers to increase the latch-up voltage or V_{BO} in the conventional CMOS-IC is to increase the effective base width of each parasitic bipolar transistor or placing the guardbands around the P-well, which indeed results in reduction of magnitudes of α's. However this approach requires extra chip areas. On the other hand, the V_{BO} can be increased by decreasing R's without **sacrificing** the packing density. The new approach can be realized by the use of the buried P^+ -well and N^+substrate in the BO-CMOS. Fig.2 shows the crosssectional view of the proposed BO-CMOS inverter. The P^+ or N^+ region provides sufficiently low base resistance R_P or R_N, which assists a rapid extraction of the excess minority carrier from each base region.

1 K bit static CMOS RAM has been redesigned by the above approach. The memory cell of six transistors has reduced to 63 % in area of the original one. The computer simulation reveals that the propagation delay at the memory cell between a word line input and the bit line output is 56 % shorter than in the conventional circuit. In the preliminary experiment, the impurity concentrations of the P^+-well and N^+ substrate are chosen so as to prevent the field inversion beneath the thick oxides, which eliminates the use of the conventional guardbands or channel-cut diffusions. The break-over and breakdown voltages of the corresponding junctions are $V_{BO} \geq 20$ v, $V_{BD1} \approx 25$ v, $V_{BD2} \approx 30$ v, and $V_{BD3} \approx 20$ v. These magnitudes are sufficient to the normal operation at 5 v supply.

Detailed fabrication prcess and pattern layout will be discussed.

References

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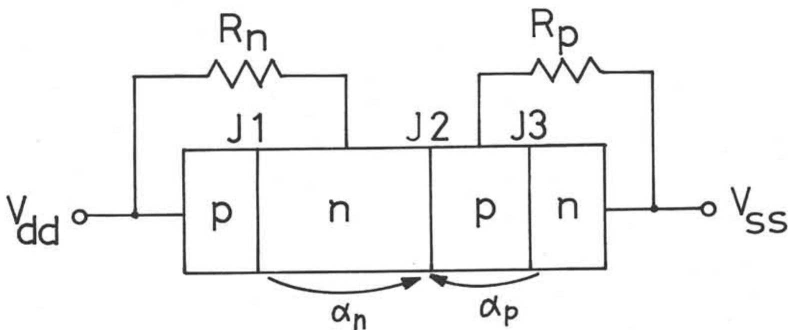

Fig.1. Shockley diode with shorted emitters for a latch-up model of CMOS-IC.

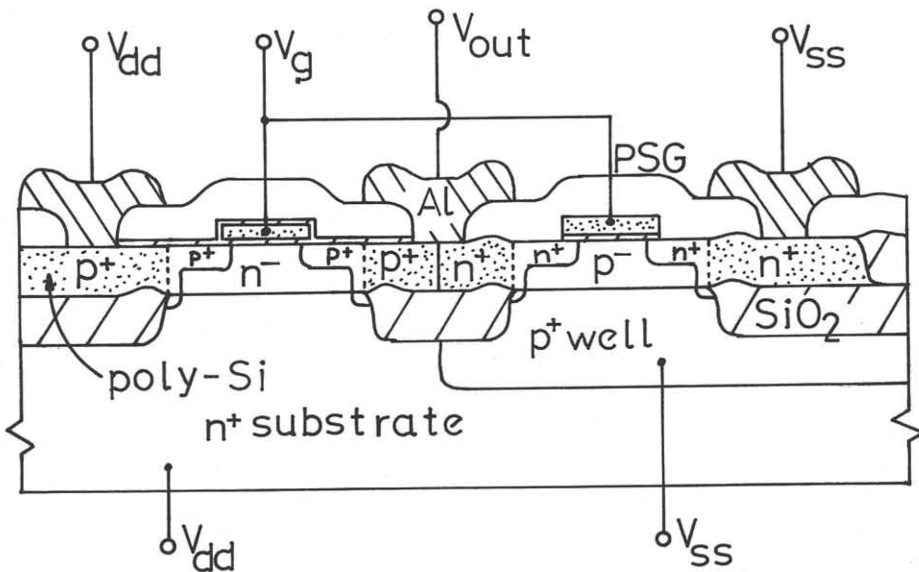

Fig.2. Crosssectional view of the proposed BO-CMOS inverter with buried P^+ layer and N^+ substrate.