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A-2-2 A 4K CMOS/SOS Static RAM with Weak Depletion Lambda Diode Cells

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This paper will report on a 4096 word by 1 bit CMOS/SOS lambda diode static RAM which is capable of data retention mode operation with less than 20 μW, and of access time of less than 65ns.

A lambda diode composed of depletion type p- and n-channel MOSFET's have been studied and reported by several authors.(1)-(3) However, the standby power was estimated to be rather high, and the access time to be long, due to a high level leakage current and limitted current drive of the diode.(3)

The RAM uses CMOS/SOS technology with single conductivity type (n^+) poly Si gate and 4 μm gate length. To minimize the leakage current of the memory cell, the lambda diode transistors are made as weak depletion type, $V_{tn\lambda}$,$V_{tp\lambda}$=0V. A load transistor is of n-channel enhancement type. The leakage current of less than 1 nA flows to maintain "1"/"0" states. Typical characteristics of the memory cell elements are shown in Fig.1. The cell consists of four transistors and the cell size is 30 x 48 μm^2.

In spite of small current drive of the cell, the column sense amplifiers, which are designed as sensitive as those of dynamic memories, enables the high speed operation of 65 ns access time. The sense circuit and the simulated wave forms of clocks are shown in Fig.2 (a) and (b), respectively. The dummy cell is composed of n-and p-channel transistors and a capacitor. The data lines are precharged via transistors Q1 and Q2, to compensate the distribution of threshold voltages of Q1 and Q2. The main sense amplifier is made of cross coupled CMOS invertors to minimize the time for the data transfer from I/0 and $\overline{I/0}$ lines to D_{out} terminal.

(1) K. Kaneko, T. Kurobe, and Y. Ogura, Meeting of Semiconductor and Transistor Groupe of Institute of Electronics and Communication Engineers of Japan, SSD-72-41(1972) (in Japanese)

(2) H. Takagi and G. Kano, IEEE J. Solid-State Circuits. SC-12,424(1977)

(3) A.C. Ipri. IEEE Trans. Electron Devices, ED-24, 751(1977)

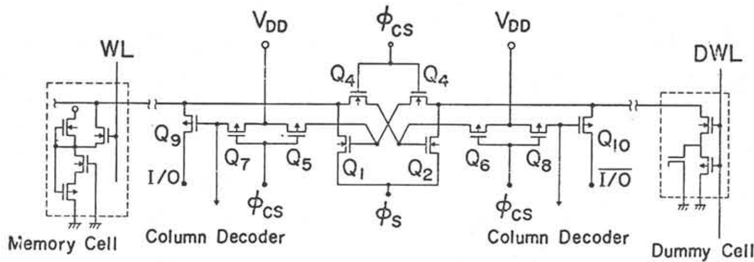

Fig. 2(a) Sense circuit.

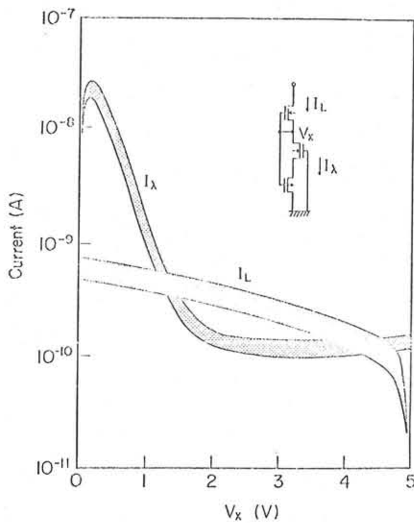

Fig. 1 Typical I-V characteristics of memory cell elements.

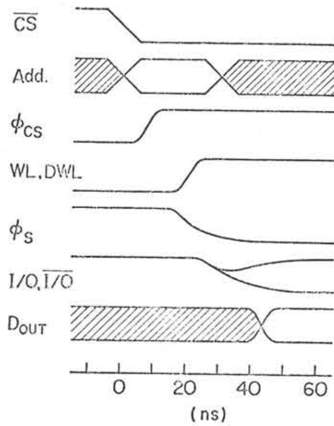

Fig. 2(b) Simulated wave forms of clocks.

Technology	Single conductivity type (n^+) poly Si gate
Chip size	3.3×4.5 mm^2
Cell size	30×48 μm^2
Access time	< 65 ns
Supply voltage	5 V
Operating power	< 95 mW @ $t_{(cycle)}$=350 ns
Standby power	< 20 μW
I/O	TTL compatible, tri-state output
Pinout	18 pin standard

Table 1 4k CMOS/SOS static RAM characteristics summary