A－2－3 A CMOS/SOS Synchronous Static RAM Fabricated with an Advanced SOS Technology

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Conventional SOS-MOS is known to have vanishingly small junction capacitance compared to that of bulk-silicon MOS if the diffusions are driven down to the sapphire.[1),2)] However, the Si-gate self-aligned technique requires the shallow junction in order to reduce the gate overlap capacitance.

An advanced technology presented in this work uses a nearly intrinsic silicon film without any process steps to dope the deep region of the film, reducing the junction capacitance even with the shallow junction. The junction capacitance is reduced because the highly resistive region of intrinsic silicon exists between the sapphire and the bases of the source and drain, as shown in Fig. 1. The localized Al penetration in device contact region causes no degradation of the device because of the high resistivity of the nearly-intrinsic film. This structure also reduces the gate capacitance when the inversion layer is not formed. The typical source-drain leak currents are 0.5 nA and 1.1 nA for n- anc p-channel MOSFET's, respectively; the channel widths of both devices are 40 μm and the channel lengths are 4 μm and 5 μm for n- and p-channel devices, respectively.

Another advantage of this technology is the simplicity of the process. It is not necessary to use the double-epitaxial process nor the ion implantation step to determine the type of the silicon film as in the conventional process[2)] in order to obtain the enhancement n- and p-channel transistors on the same chip. Figure 2 shows that the enhancement mode n- and p-channel MOSFET's can be obtained on the intrinsic SOS films. Threshold voltages shift toward more enhancement mode bias voltages as the silicon film thickness decreases. This phenomenon is explained by the model of the deep defect levels in the film.[3)]

Figure 3 shows the photomicrograph of the fabricated CMOS/SOS synchronous static 1 k-bit RAM with this advanced technology of 0.6 μm thick silicon film, 600 Å thick oxide and the ion-implanted shallow junctions. The RAM is fabricated also on the bulk silicon by using the same mask patterns. The above oxide thickness is chosen by the computer simulation. The simulated access times of both SOS and bulk LSI are shown in Fig. 4. The access times of SOS are short due to the small parasitic capacitance. As X_{ox} decreases, the access time of the bulk LSI becomes short due to the decrease of the weight to the parasitic capacitance, but those of the SOS-LSI increases at $X_{ox} < 500$ Å resulting from the increase of the gate overlap capacitance. Figure 5 shows that the access time on the SOS is faster than

that on the bulk silicon by a factor of 1.5 at the same power supply voltage V_{CC}. The shortest access times on the SOS are 40 ns at V_{CC} = 5 V and 20 ns at V_{CC} = 10 V. Figure 6 shows the waveshapes of the chip enable input and the data output signals with typical access time of 55 ns at V_{CC} = 5 V. The average supply currents of 0.74 mA are measured at the cycle time of 1 μs and V_{CC} = 5 V; this active power dissipation is 65 % of that on the bulk silicon. The quiescent powers on the SOS are obtained as 0.3 mW at V_{CC} = 5 V.

References

1) S.S.Eaton, Electronics, June 12 (1975) 115.
2) A.Capell et al., Electronics, May 26 (1977) 99.
3) N.Sasaki and R.Togei, to be published.

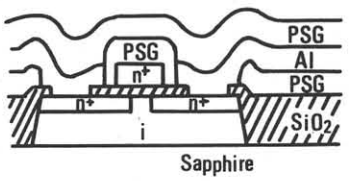

Fig.1 Cross section of the MOSFET.

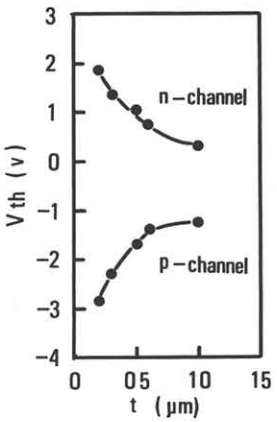

Fig.2 Threshold voltage of SOS-MOSFET's on the intrinsic film as a function of the silicon film thickness t; the gates are doped n-type.

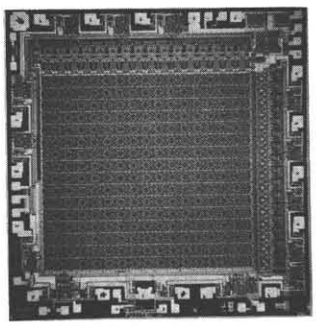

Fig.3 Photomicrograph of the synchronous static CMOS/SOS RAM.

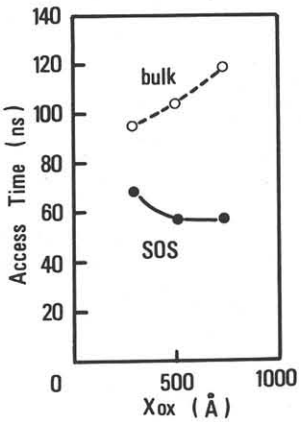

Fig.4 Simulated access times of the SOS and bulk-silicon RAM's as a function of the gate oxide thickness X_{ox}. V_{CC} = 4.4 V.

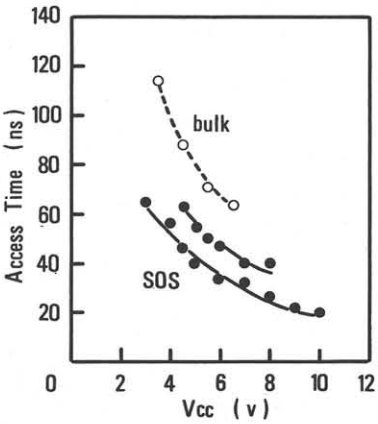

Fig.5 Access times of the fabricated SOS and bulk-silicon RAM's.

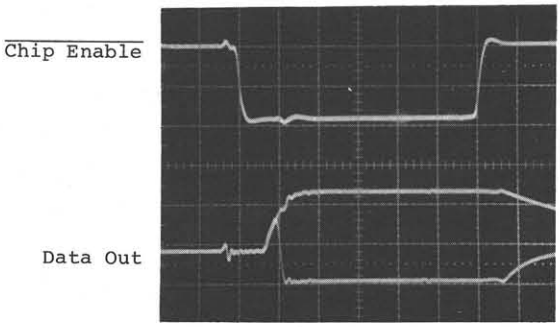

Fig.6 Oscillograph of SOS memory access time from chip enable; V_{CC} = 5 V. (Horz. : 50 ns/div., Vert. : 2 V/div.).